On-chip ESD solutions seminar

MAY 6, 2015 – SHANGHAI

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Sofics is a foundry-independent IP provider

- Semiconductor IP provider
  - Sofics = “Solutions for ICs”
  - IP portfolio
    - Since 2000: On-chip ESD protection for CMOS, SOI applications up to 5V
    - Since 2010: On-chip ESD protection for applications 5V to 100V
  - New (non-ESD) portfolio’s under development
- Consulting
  - On-chip ESD protection support
- Test lab
  - ESD relevant analysis
  - Transmission Line Pulsers, HBM, MM, Latch-up, IEC 61000-4-2

Outline

- Introduction
  - Reason for On-chip ESD protection
  - ESD design window
  - ESD protection concepts
- ESD protection for advanced CMOS
- ESD protection in high voltage, BCD
- ESD protection in SOI technology
- Summary, conclusions

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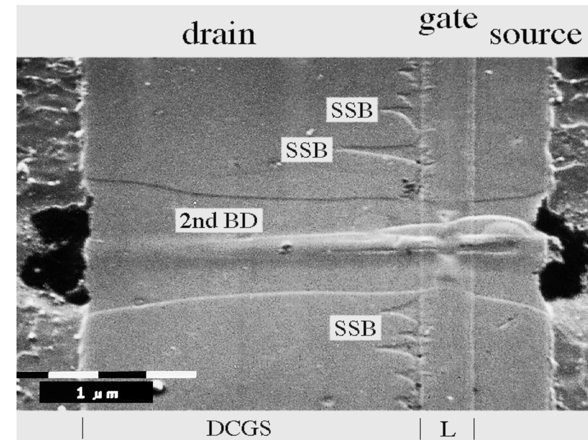
What is ESD?

- What is Electrostatic Discharge ('ESD')?
  - The sudden discharge of a charged body
    - Short time (<1us)
    - Short rise time (<10ns)
    - High current levels (1-10A)
      - and beyond...
  - Tribo-electric and induced charging
- Damages caused by
  - Charged Human
  - Charged machinery/robotic
  - Charged IC's

Description	Typical voltage (V)
Person walking over carpet	15.000
Person working at a table	800
Circuits after removing protective foil	20.000

What is ESD? – Importance for IC industry

- Importance of ESD for IC industry
  - Occurance of ESD events
    - Wafer fabrication, testing, dicing
    - Packaging, assembly, testing
    - IC transportation
    - Board level assembly, testing
    - System level assembly, testing
    - Functional use of systems
  - Silicon melting, junction or gate breakdown
  - Industry quotes about ESD failures:
    - “Responsible for 20-30% of IC failures”
    - “25.8% of the products rejected”
    - “Estimated 8 to 33% of all product losses”



Solving Electrostatic Discharge

- Solving ESD issues
  - Prevention of charge build-up
    - Fab level: air ionizers
    - Proper grounding methods during handling, packaging, testing, shipping
    - Dissipative materials
  - Modification of process technology
    - Build-in ESD robustness to the transistors
  - Protection
    - Device Level: On-chip protection design at the signal/supply pins
    - System level: transient suppression elements

What to do about ESD?

Anti-static and conductive packaging

WRIST STRAP

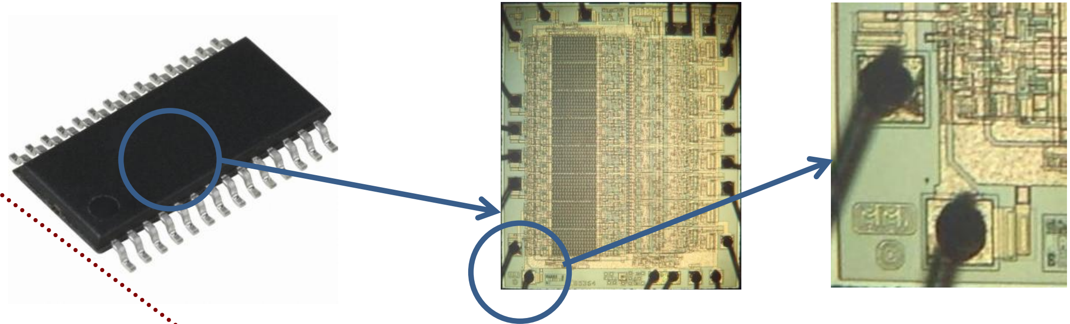
IONIZERS: ground connection is not always possible: reduce insulation property of air

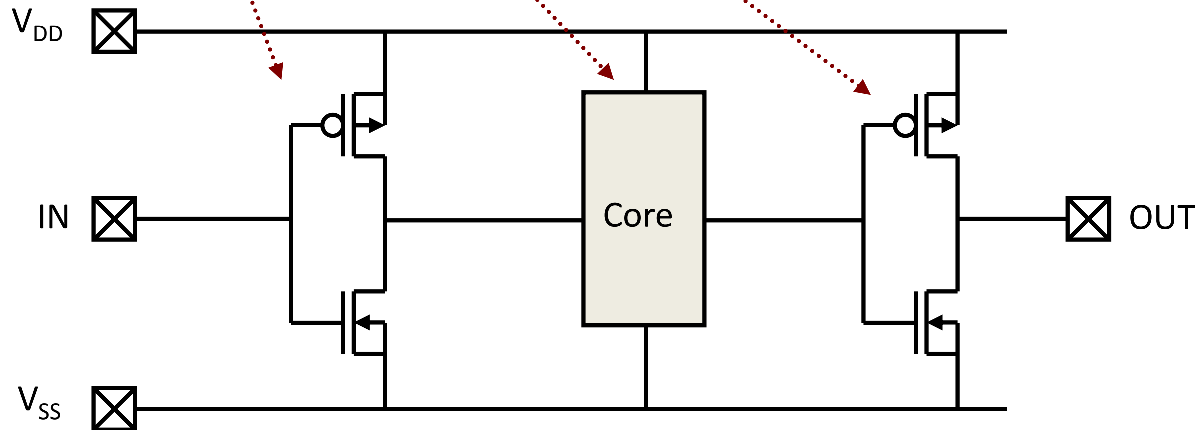
HEELSTRAPS: Discharge path in combination with conductive floor

Anti-static + grounded workdesk

What is ESD? - In the IC world

- ESD stress applied to IC circuits can introduce damages
  - Output drivers
  - Core elements
  - Input circuits





Solution: on-chip ESD protection

- On-chip ESD protection
  - ESD clamp/diode devices at IO interfaces, power pads
  - Different concepts are used in the industry

V_{DD}
IN
V_{SS}
Core
OUT

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- **Introduction**
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  - **ESD design window**
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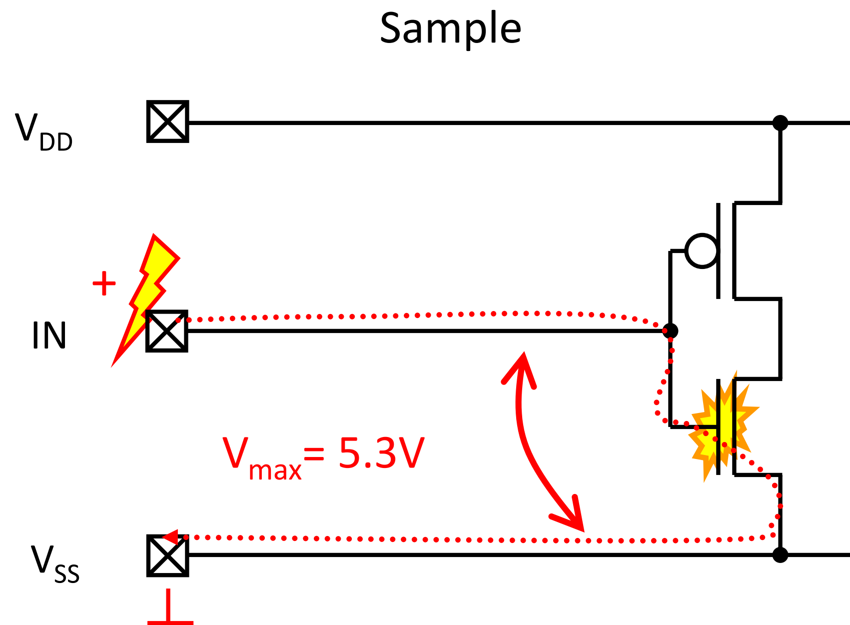
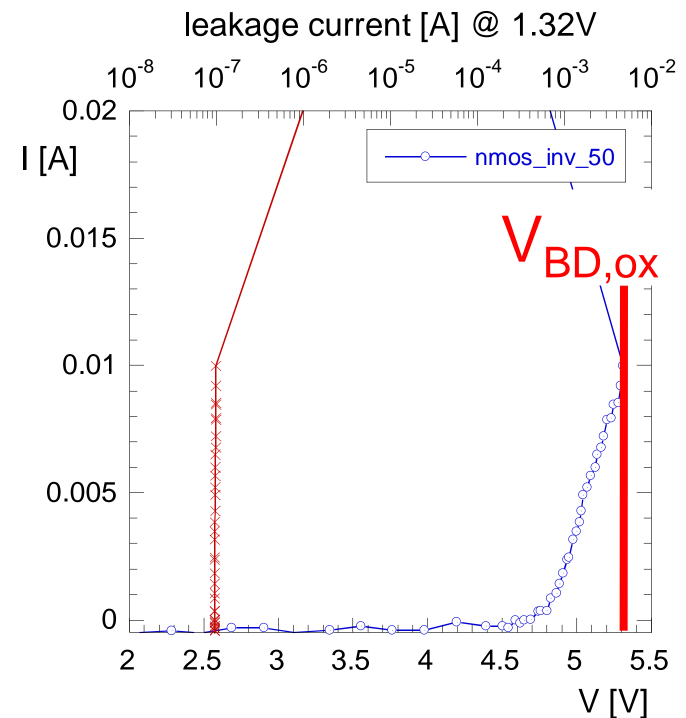
How to deal with ESD? - ESD “switches”

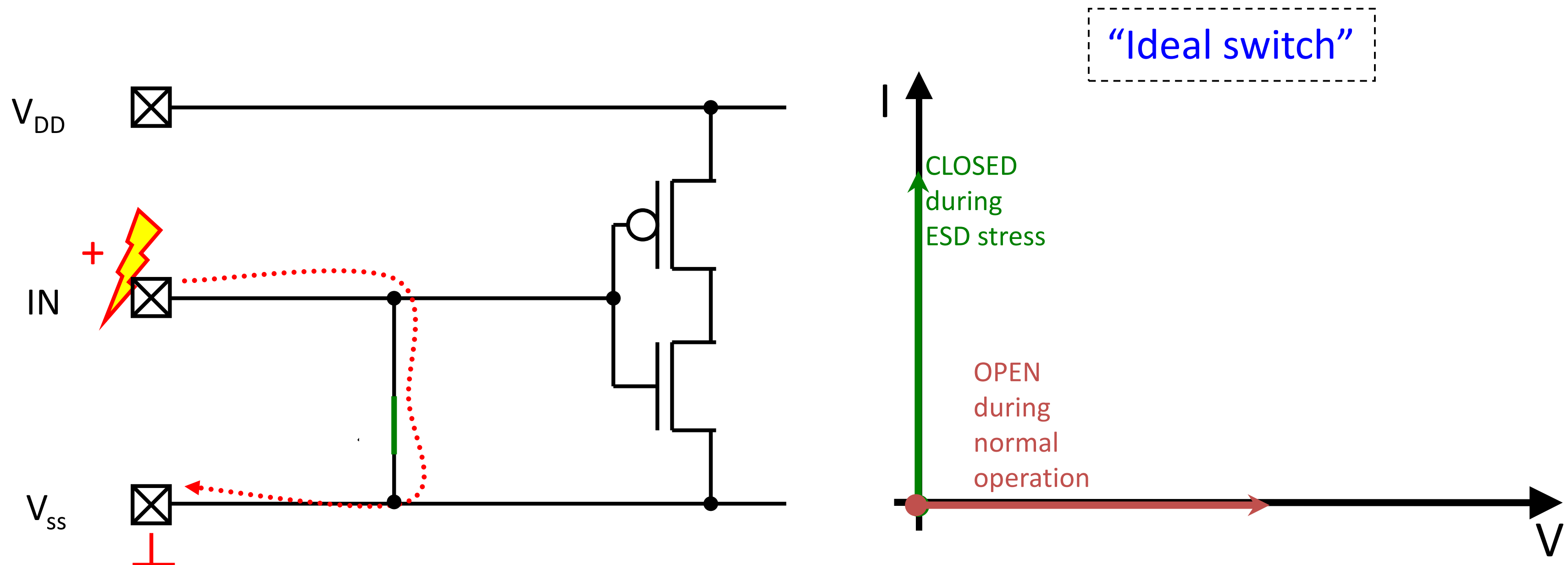
- ESD stress example: **input** circuit
  - Problem: gate oxide breakdown
    - Voltage between IN-V_{SS} above gate oxide breakdown voltage ($V_{BD,ox}$)





How to deal with ESD? - ESD "switches"

- ESD stress example: **input** circuit
  - Problem: gate oxide breakdown
  - Solution: create a parallel low-ohmic current path to shunt the ESD current, " a switch"



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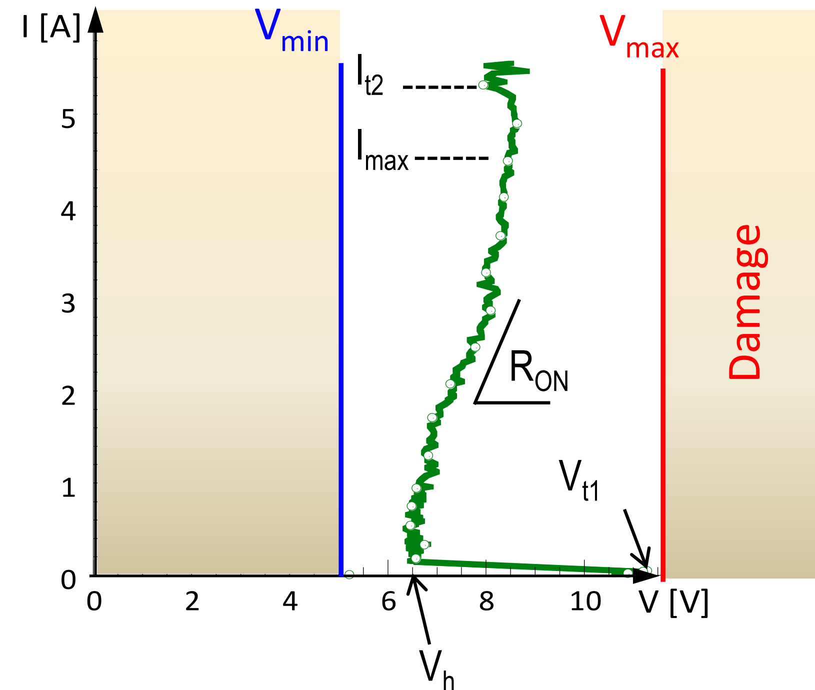
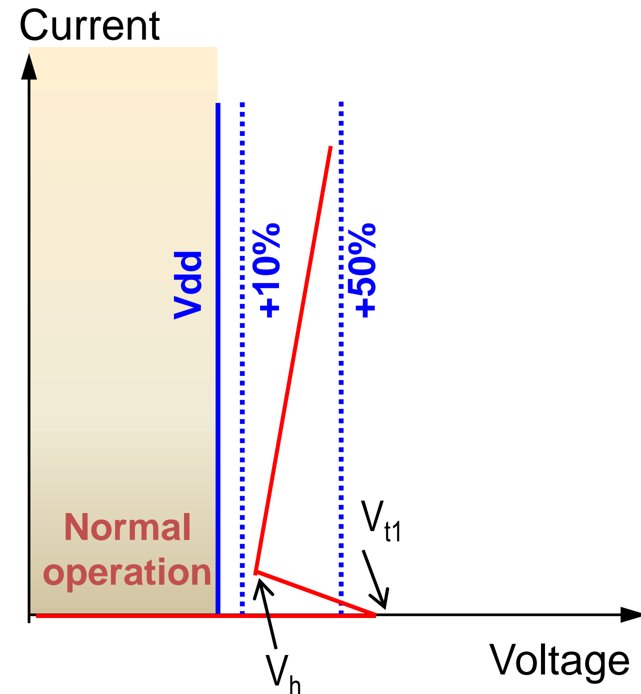
How to deal with ESD? - ESD "switches"

- Non-ideal ESD switch
  - Influence on normal operation
    - Leakage
    - Capacitance
  - Trigger voltage (V_{t1})
  - Finite turn-on time
  - Holding voltage (V_h)
  - Dynamic series resistance (R_{on})
  - Limited current capability
    - I_{t2} – failure current
    - I_{max} – maximum current (including safety margin)



How to deal with ESD? - Design window

- Requirements for ESD protection switches – TRANSPARENT
  - Invisible during normal operation
    - Low leakage
    - Low capacitance (speed!)
    - No LU issues
    - Normal operation region is defined by:
      - V_{t1} requirement for burn in and LU test: **V_{DD} + 50%**
      - V_h requirement for LU test: **V_{DD} + 10%**



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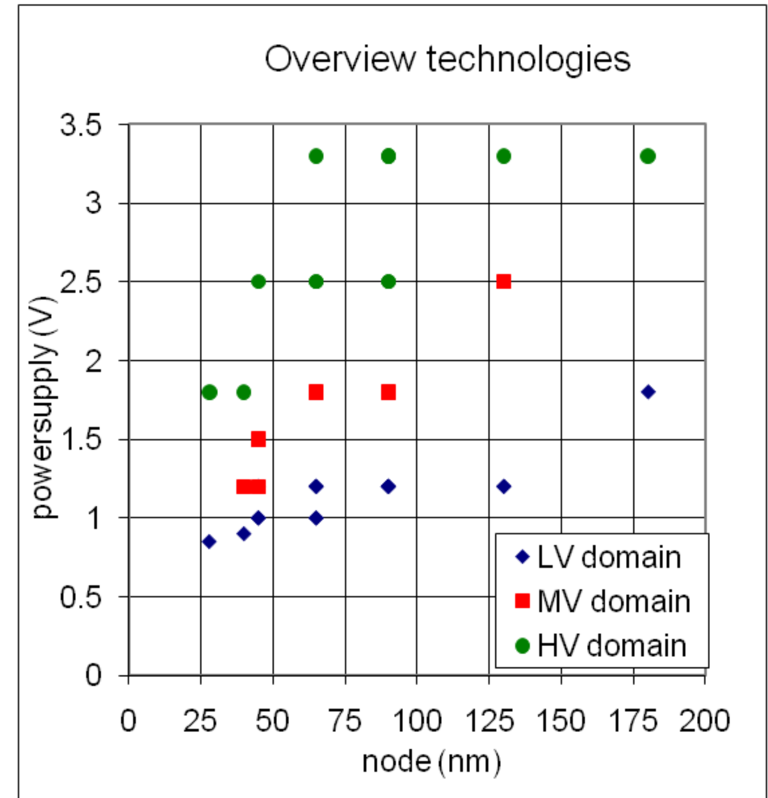
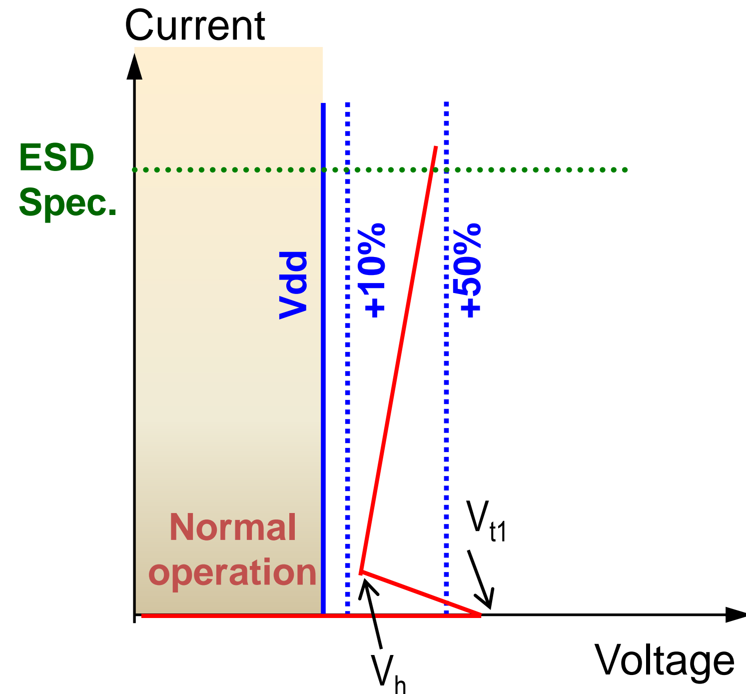
ESD design window

- Data collected from **different** CMOS technologies
  - From **0.18um** down to **28nm**
    - **23** different technologies
    - Different Chip manufacturers
  - Bulk CMOS
  - Vdd levels decreasing

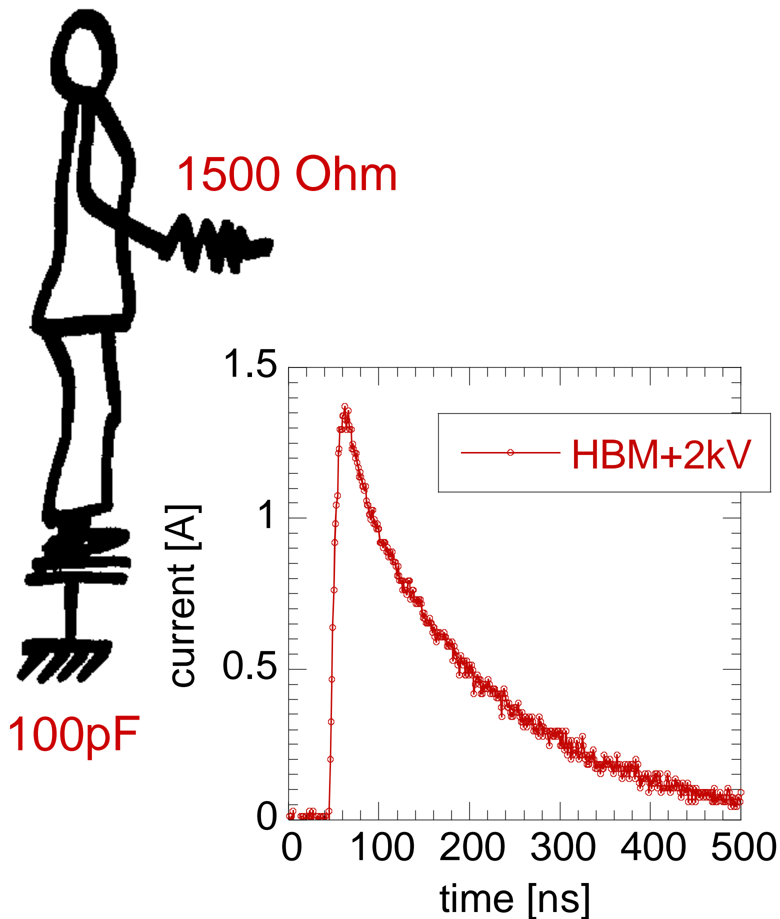


How to deal with ESD? - Design window

- Requirements for ESD protection switches – ROBUST
  - Protection strength during ESD operation
    - Large current shunting capability
      - ESD current level specification
  - Certain current level
    - Related to field failures?
  - Different models developed
    - Human Body Model ('HBM')
    - Machine Model ('MM')
    - Charged Device Model ('CDM')
  - Analysis tool
    - Transmission Line Pulser ('TLP')

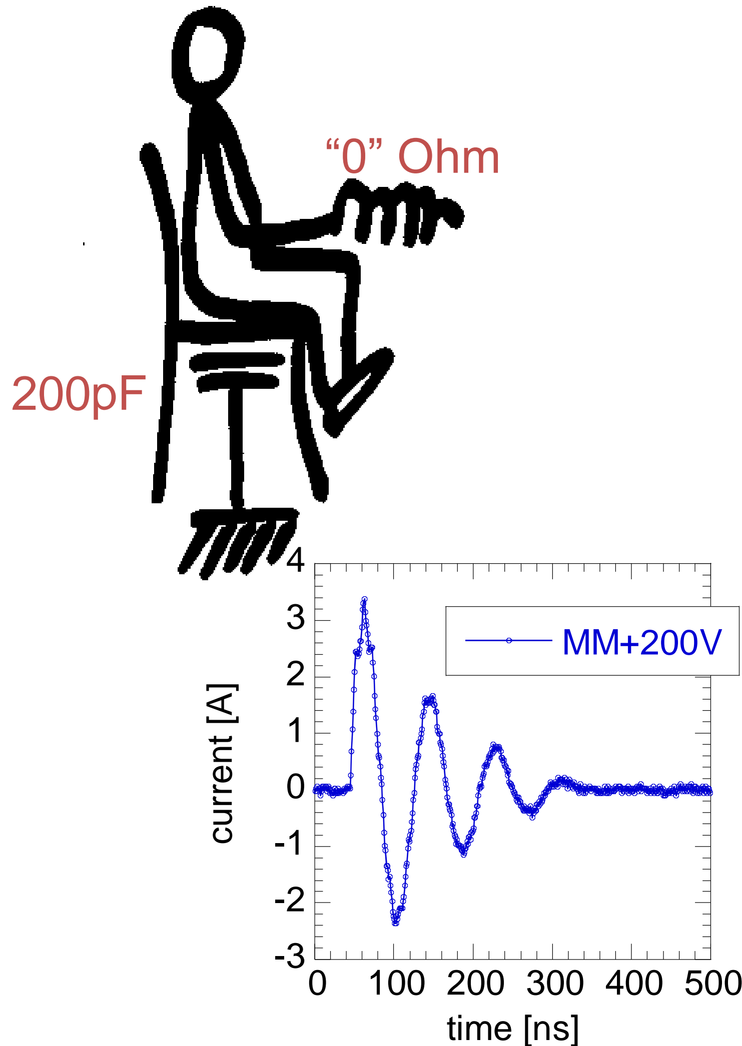


Human Body Model - HBM



- HBM
  - Modeled by a network of a 100pF capacitance discharging through a 1500 Ohm resistor.
  - Represents the discharge of a **standing individual** through a pointing finger.
  - Acts as a current source, **forcing current from external** through the IC.
  - **Stress applied between 2 IC pins** (stress pin and ground pin).

Machine Model - MM



- MM
  - Modeled by a network of a 200pF capacitance discharging through a 0 Ohm resistor, and some inductance.
  - Represents the discharge of a **sitting individual through a metal/low resistive tool**.
  - Acts as a current source, **forcing current from external** through the IC.
  - **Stress applied between 2 IC pins** (stress pin and ground pin).

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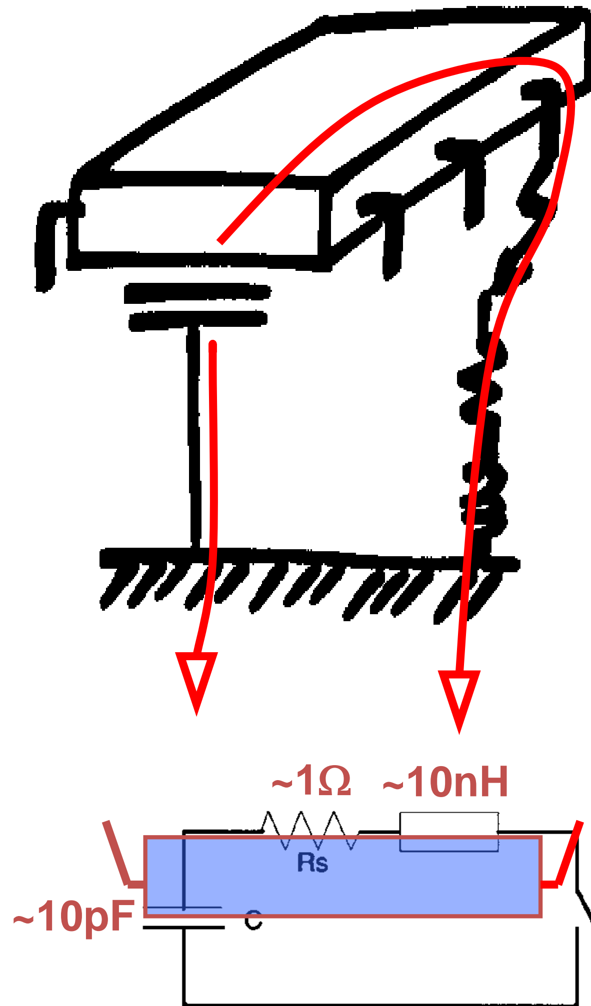
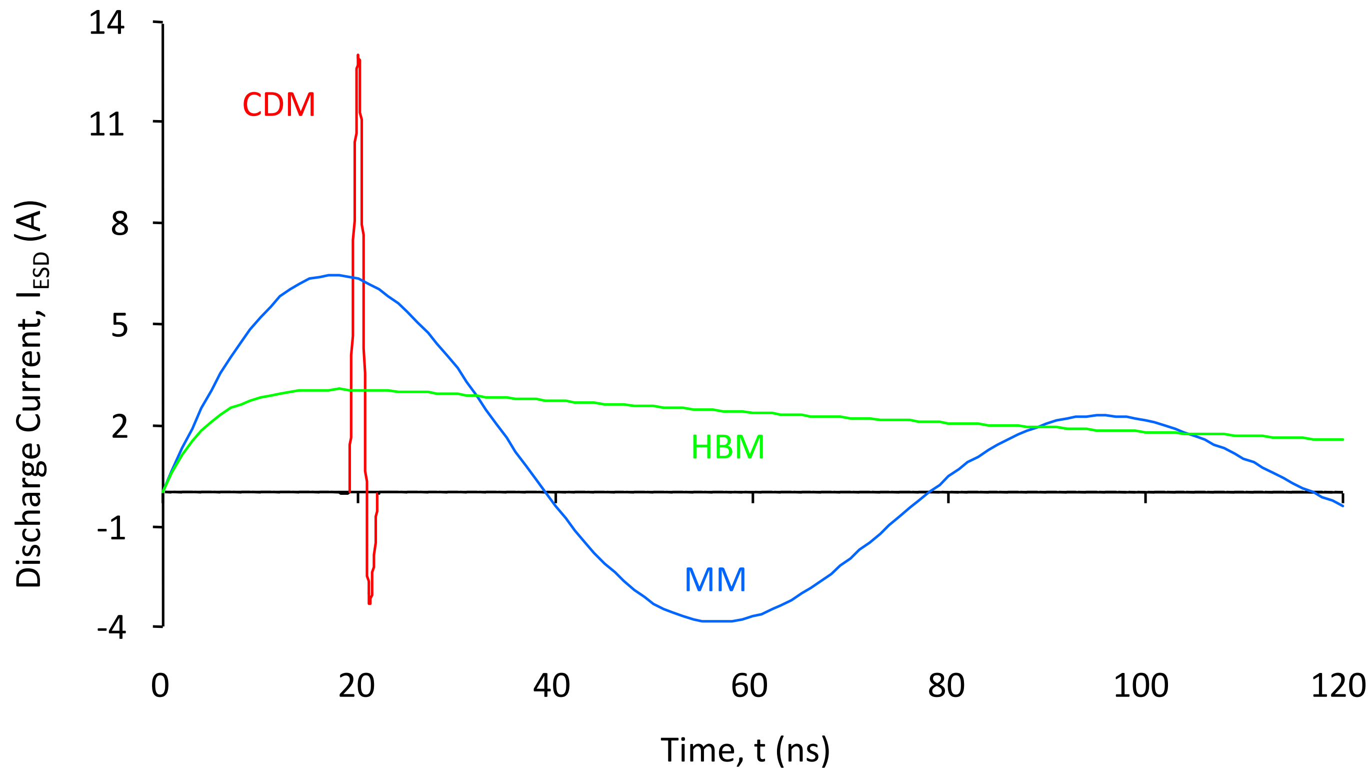
Charged Device Model - CDM



- CDM
  - Modeled by a network consisting of the IC capacitance to ground, discharging through an arc, which forms a non-linear, time variant resistance and inductance.
    (LC dominated model with small C)
  - Represents the discharge of charged IC to ground.
  - Acts as a current source, **forcing current from internal out of the IC to ground**, while a complementary current flows outside the device to close the current loop.
  - **Stress applied to one IC pin**

ESD Waveforms Comparison

HBM vs CDM vs MM
(5000V) (500V) (500V)



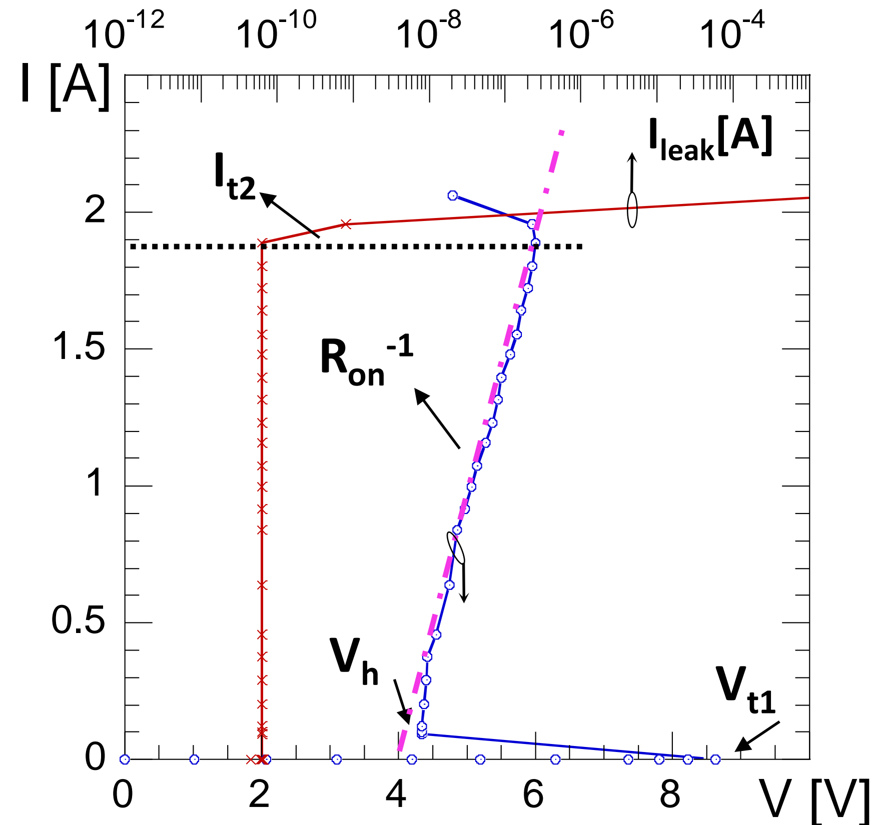
Courtesy of
Horst Gieser

ESD models Comparison

Model	HBM	MM	CDM
Pulse width [ns]	~150	~80	~1
Rise time [ns]	2-10	~ 20	<0.4
Typical ESD failures	▪ Junction damage ▪ Metal penetration ▪ Metal melt ▪ Contact spiking ▪ Gate oxide Damage		▪ Gate oxide damage ▪ Charge trapping ▪ Junction damage

a typical TLP characteristic

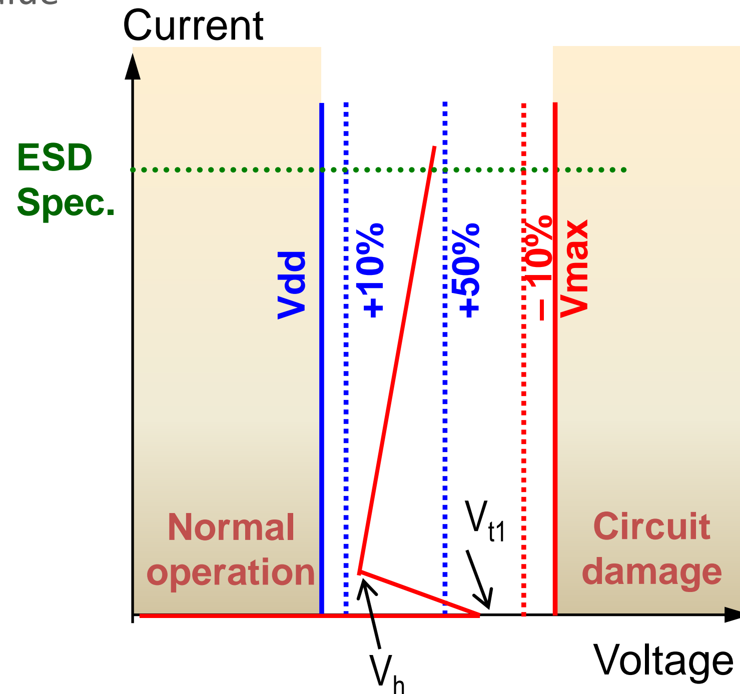
- No conduction until **trigger voltage V_{t1}** is reached
- Snapback to **holding voltage V_h**
- Conduction up to **failure current I_{t2}** or failure voltage V_{t2}
  - with a specific **on-resistance R_{on}**
    - $V=V_h+R_{on}\times I$



- Alternative situations
  - No snapback: $V_h=V_{t1}$
    - e.g. diode in forward
  - No conduction: $I_{t2}=0$; $V_{t1}=V_{t2}$
    - e.g. gate oxide

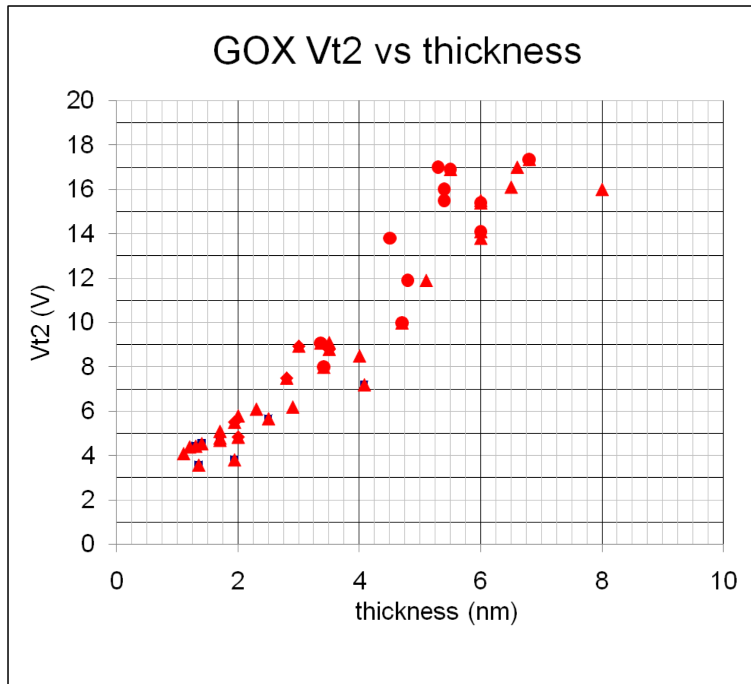
How to deal with ESD? - Design window

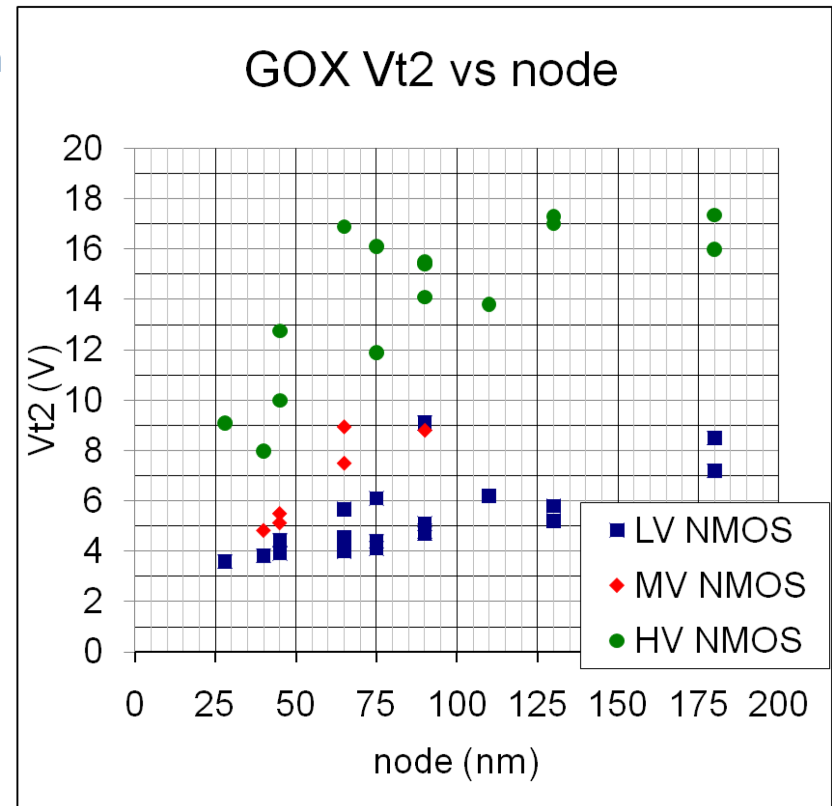
- Requirements for ESD protection switches – EFFECTIVE
  - Protecting during ESD
    - Effective: clamping voltage to safe value
      - V_{max} defined by sensitive element:
        - Core
        - GOX
        - MOS devices
      - $V_{t1} < V_{max} - 10\%$



ESD design window Vmax – Gate oxide failure

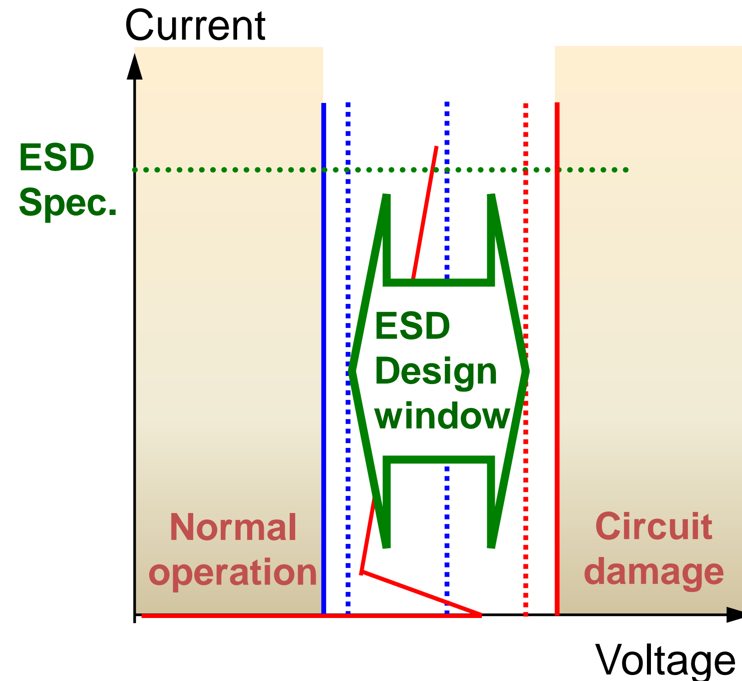
- Gate oxides become thinner
  - **Decrease in thickness** from more than 4nm to 1.3nm in 28nm (LV domain)
  - **Decrease of failure voltage** from 8.5 V to 3.85 V (LV domain)





How to deal with ESD? - Design window

- Summary of the requirements for ESD protection switches.
  - Invisible during normal operation
    - Low leakage
    - Low capacitance (speed!)
    - No latch-up (LU) issues
  - Protecting during ESD
    - Robustness: Large current shunting capability
    - Effectiveness: clamping voltage to safe value



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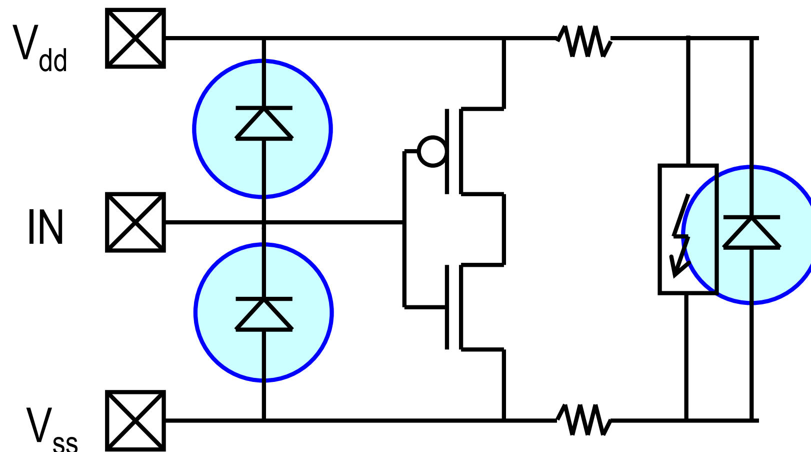
ESD protection devices and concepts

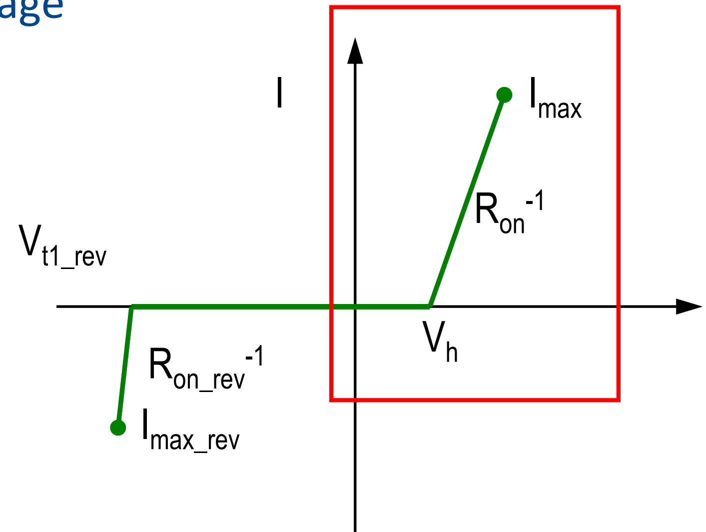
- **Level 1: Devices: basic 'building blocks' or ESD devices?**
  - **Diodes**
  - **Snapback MOS / bipolar devices**
  - **Active mode MOS device**
  - **Silicon Controlled Rectifiers ('SCR')**

- Level 2: Protection concepts: arranging devices into protection circuits?
  - Dual diode
  - Self protective drivers
  - Full local protection
  - Secondary protection approach

Basic ESD elements: Diodes - use

- **Forward mode diodes** are used for ESD protection
  - Dual diode approach for IO's
    - Diode down between Vss and IN/OUT
    - Diode up between IN/OUT and Vdd
  - Diode between Vss and Vdd
  - Trigger circuits (see further)
  - Holding diodes for increased holding voltage



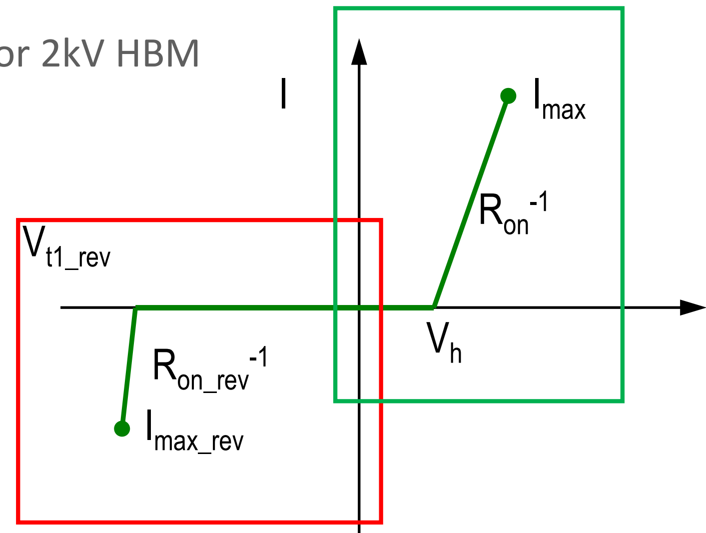


Basic ESD elements: Diodes – Typical values

- Typical values
  - Forward conduction
    - Imax = ~ 35 mA/um
    - Example: 40um diode width required for 2kV HBM (~1300 mA)
    - Vh = 0.7V
  - Reverse conduction
    - Imax = ~ 0.3 mA/um
    - Example: 4500um diode width required for 2kV HBM
    - Vt1_rev is process dependent

      = function of (Anode, Cathode doping)

      = function of Anode Cathode spacing



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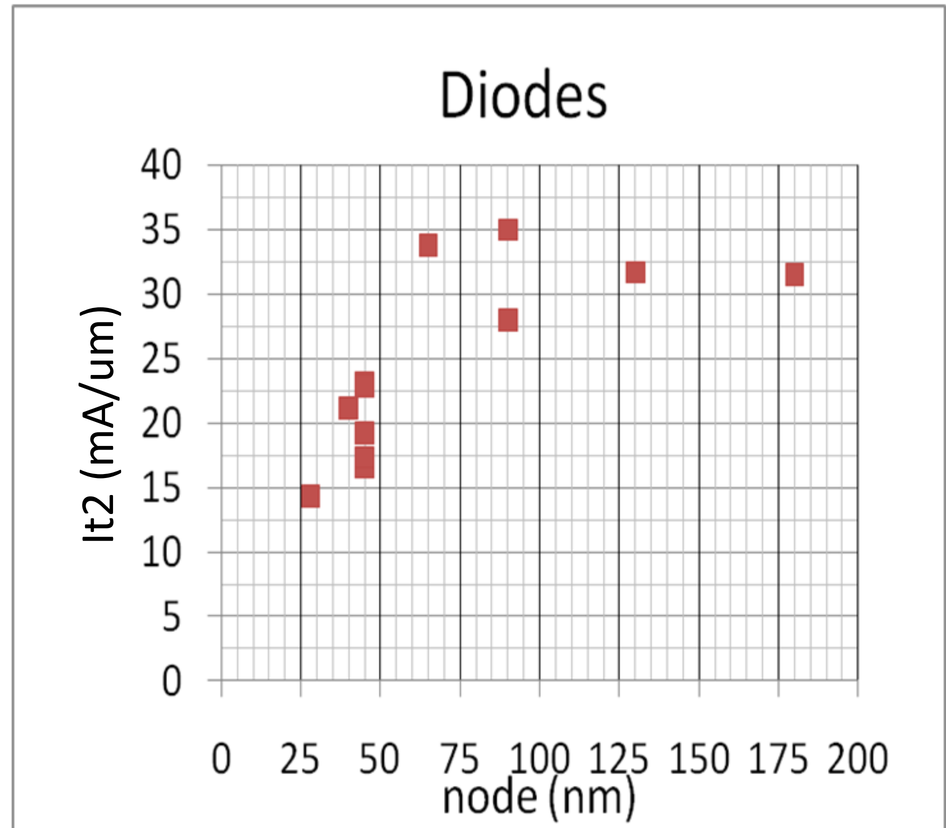
SOFICS Solutions For ICs

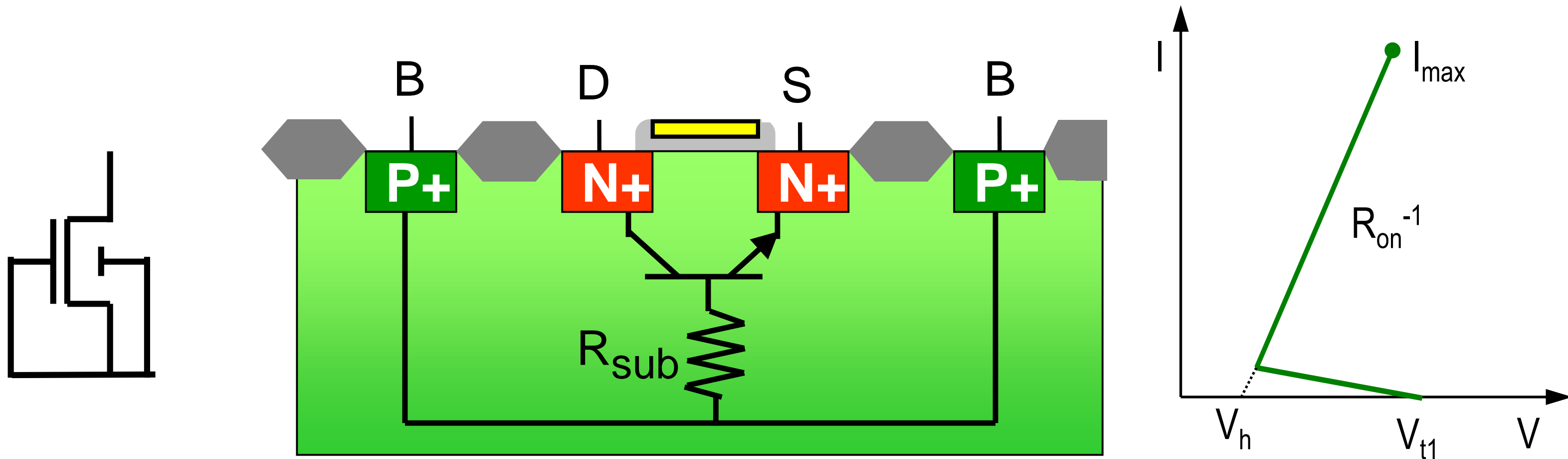
Diode trends

- Diode ESD performance
  - 35mA/um up to 65nm
  - Drop in performance in 40nm, 28nm



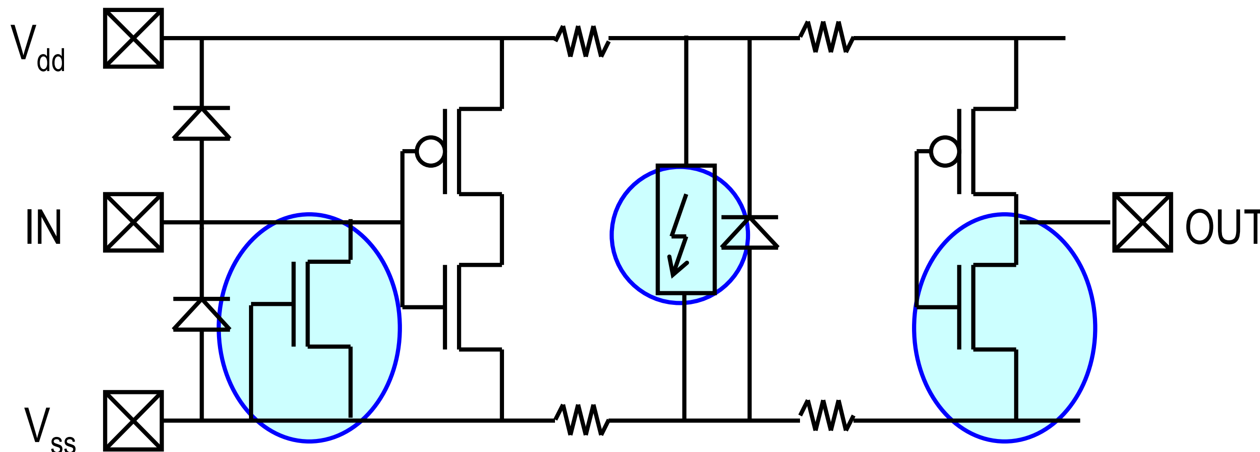
Basic ESD elements: snapback ggNMOS

- Snapback NMOS
  - Schematic
  - Cross section: parasitic NPN device
  - Characteristic behavior
    - Snapback curve
    - Turn-on of parasitic bipolar device



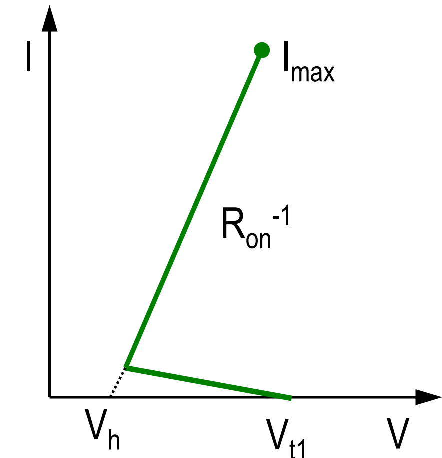
Basic ESD elements: ggNMOS - use

- **Snapback mode NMOS** is used for ESD protection
  - Power protection between Vdd and Vss
  - Local protection for input: Mature & HV CMOS nodes
  - Self protective output drivers
  - Trigger element for other ESD clamps
  - **Low voltage, mature (>0.18um) nodes: ggNMOS is very good solution!**



Basic ESD elements: ggNMOS – Typical values

- Typical values for ggNMOS
  - Imax = ~ 7 mA/um
    - Example: 200um width required for 2kV HBM (~1300 mA)
  - Vt1
    - Process dependent (doping levels)
    - Examples:
      - Vt1 = 5V for 65nm – GOX1
      - Vt1 = 10V for 0.35um
  - Vh
    - Process dependent (doping levels)
    - Function of the gate length ('Lg')
    - Examples:
      - Vh = 3V for 65nm – GOX1
      - Vh = 5V for 0.35um



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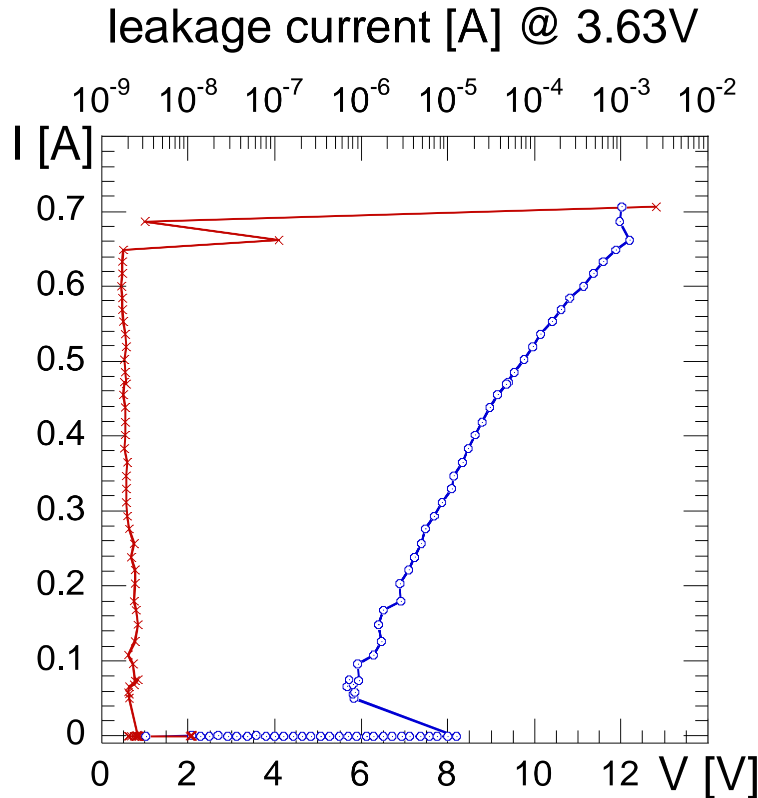
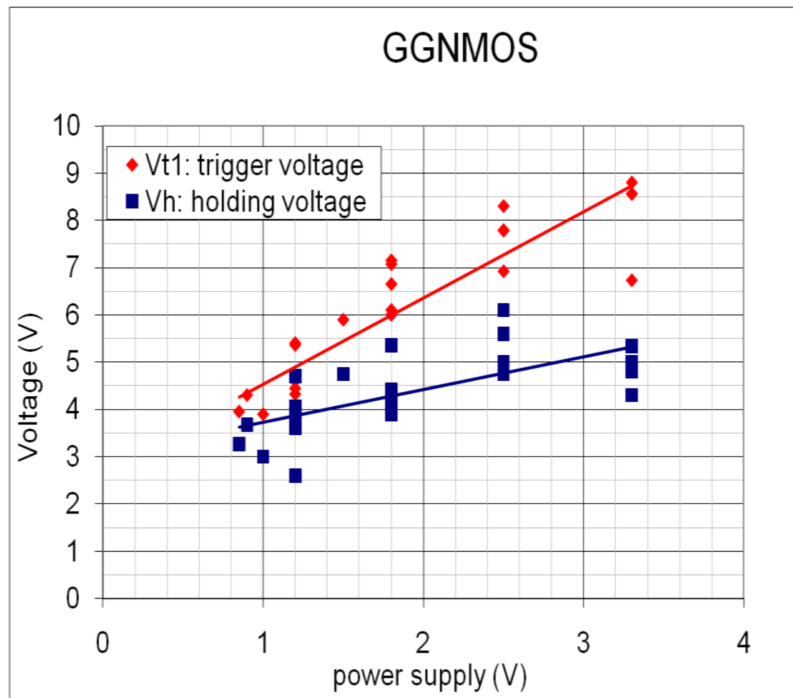
Basic ESD elements: ggNMOS

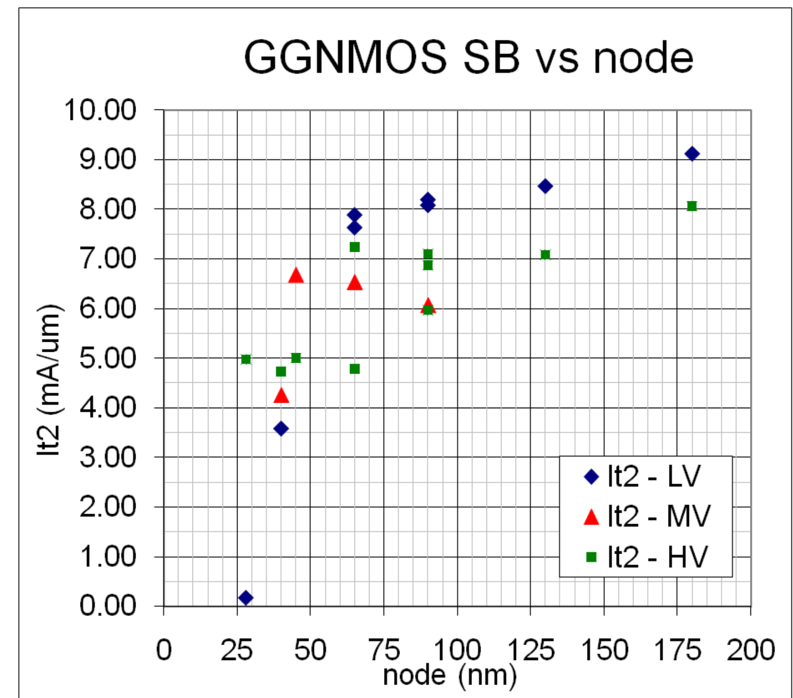


- Advantages
  - NMOS is standard device
  - Moderate Current capabilities
    - Mature technologies: > 10-15 mA/um
    - Advanced techn: 5-7mA/um
  - Typically no latch up risk
- Disadvantages
  - Does not work in HV technologies
  - Fairly large devices needed
  - Not applicable for advanced technology nodes (~ < 90nm)

Snapback NMOS performance trends

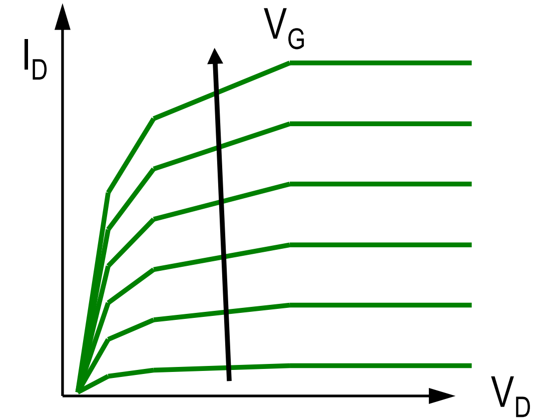
- (GG)NMOS: stronger decrease in performance for 65nm and below
  - 28nm: SB GGNMOS **does not survive snapback**



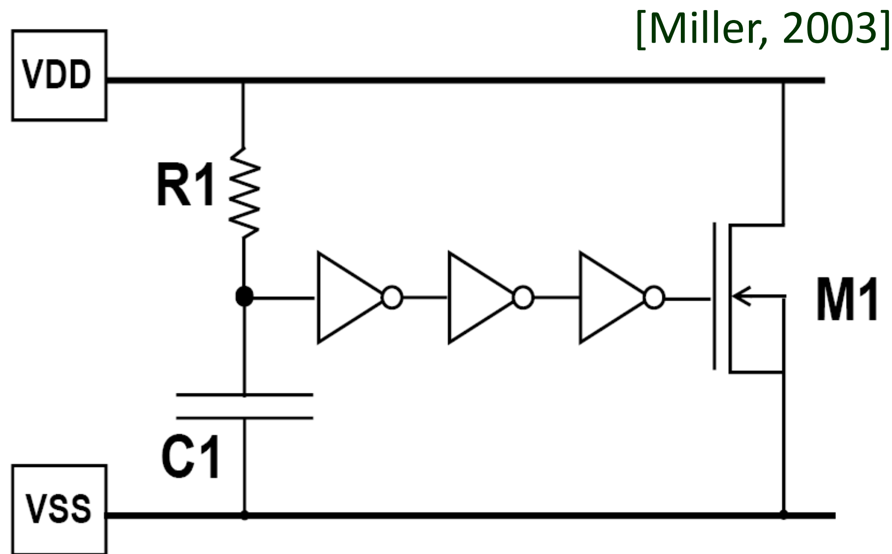


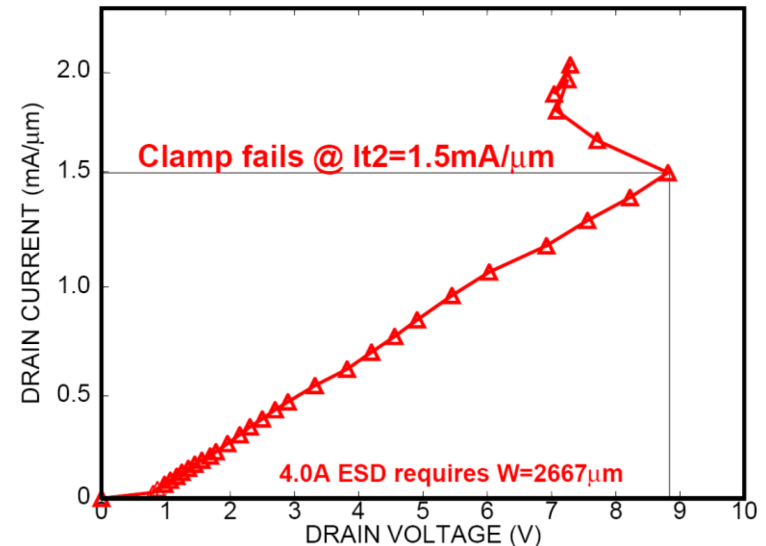
Basic ESD elements: Active mode MOS

- Active mode MOS: No snapback
  - Schematic (Basic scheme)
  - Characteristic behavior
    - NO Snapback
    - MOS mode operation
    - Dynamic triggering

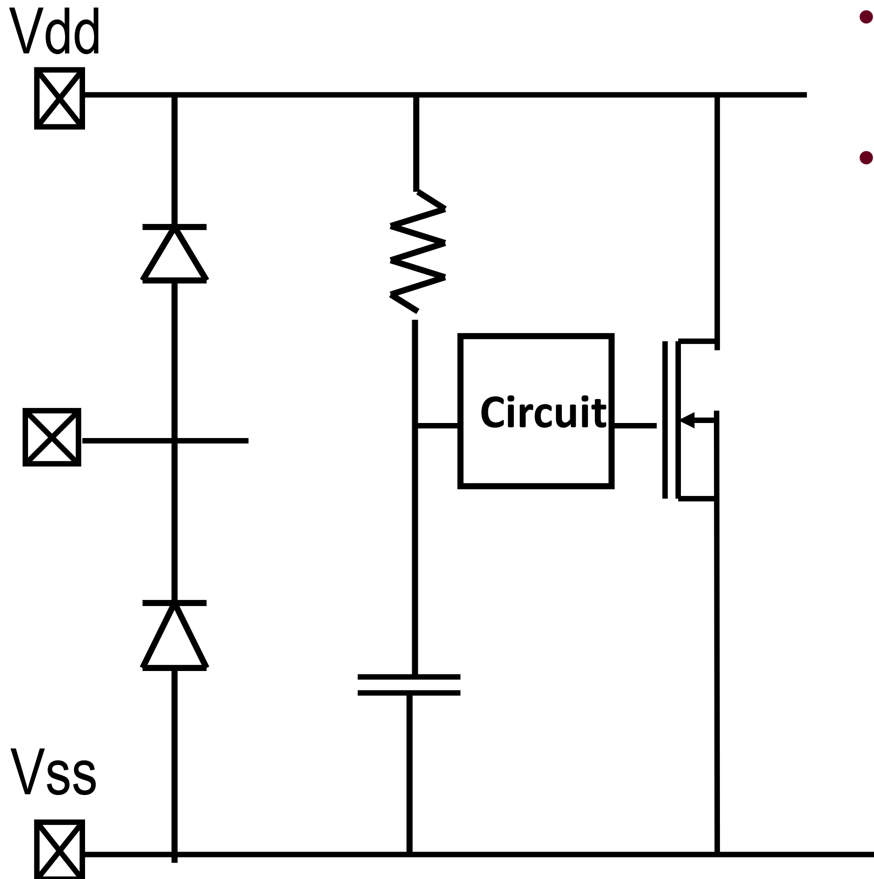


[Miller, 2003]





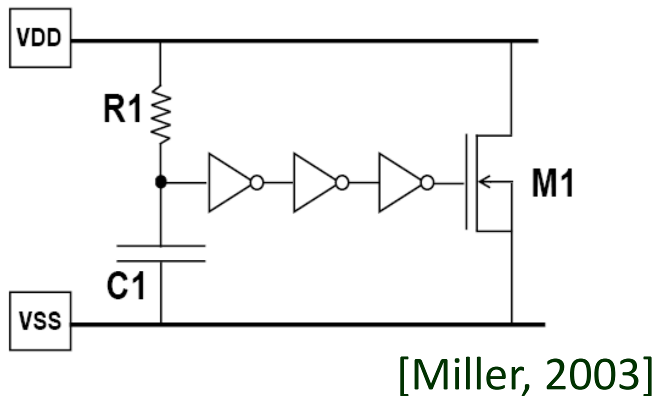
Protection Devices - Active MOS device



- A railclamp is placed between power and ground potentials
- The elements of a railclamp are:
  - RC time circuit to detect ESD
    - Few ns needed to detect ESD
    - ~us to keep signal to MOS gate
  - Large MOS device to shunt ESD current
  - Circuit is added for
    - Improved noise immunity
    - Allowing smaller timeconstants

Different approaches - improvements

- Conventional triggering
  - Single time constant
  - Large layout area for R1, C1
  - Susceptible for false triggering
- Improved Trigger scheme
  - Dual time constants
  - Separate ESD detector and on-time delay
  - R1,C1 filter tuned to ESD rise time (~40ns)
  - R2,C2 tuned for ~1us on-time during ESD



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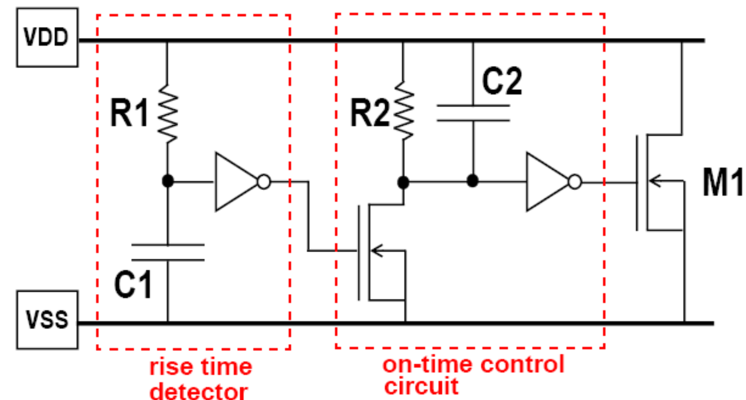
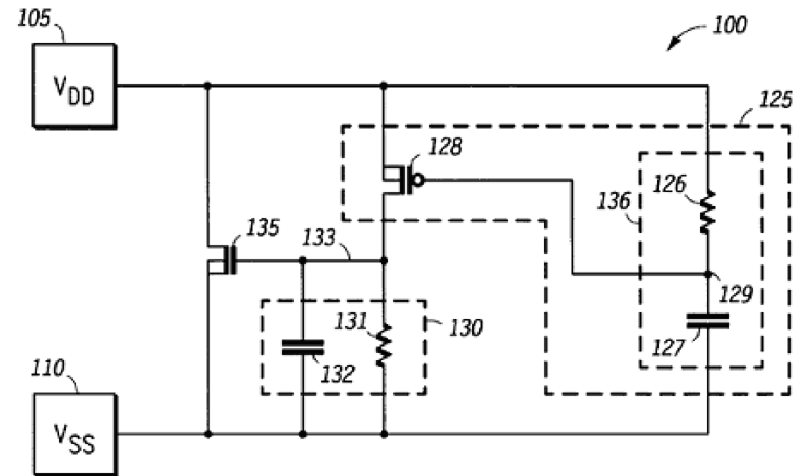
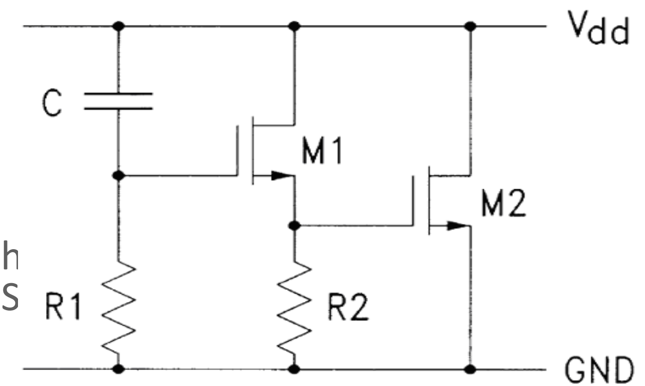


Many companies use BIGfet applications

- Many companies use BIGFET
  - Motorola / Freescale
    - Distributed versions
  - National Semiconductor
    - Merrill clamps
  - Intel
    - PMOS based clamps
    - Low leakage versions
  - Texas Instruments
    - Feedback mechanisms to reduce area
  - Others
    - Focus on reducing area for R,C
    - Winbond Electronics, Infineon Technologies, Harris Corporation, Analog Devices, Lucent Tech HP, Cirrus Logic, Western Digital, AG, Compaq, S

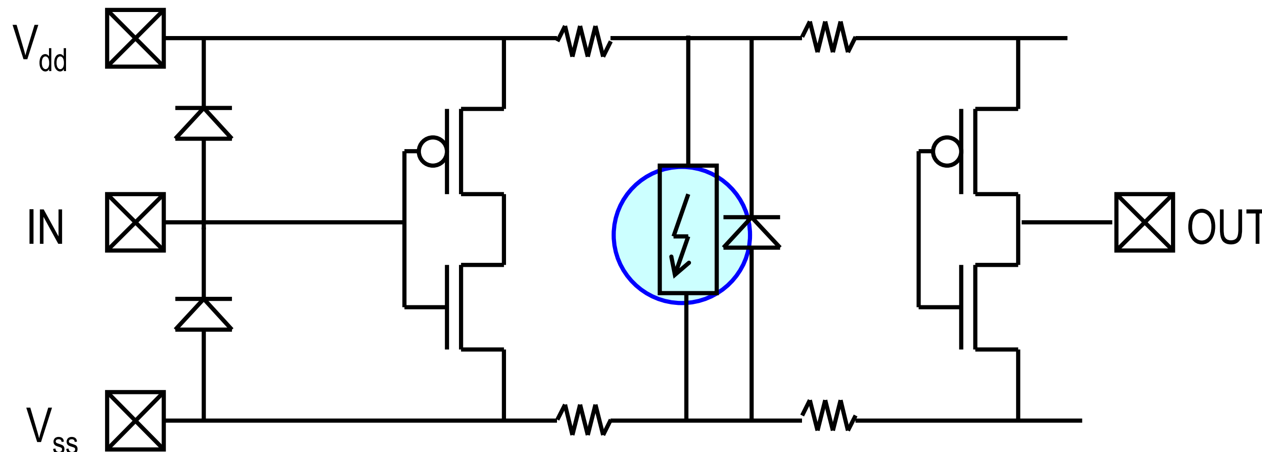




Basic ESD elements: Active MOS - use

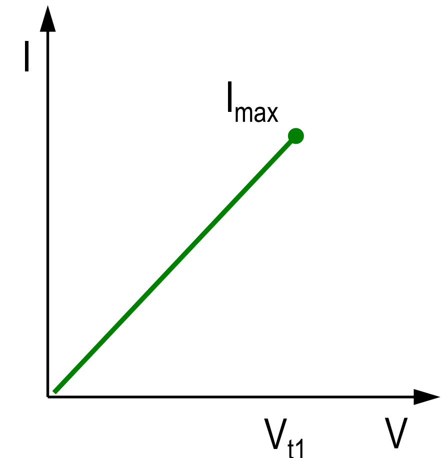
- **BIGFET mode NMOS** is used for ESD protection
  - Power protection between Vdd and Vss

  - **BIGFET is good solution for mature nodes**
  - **BIGFET is difficult for advanced technologies, thin oxide IO protection**



Basic ESD elements: Active MOS – Typical values

- Typical values for BIGFET
  - Imax = ~ 1 mA/um
    - Example: 1300um width required for 2kV HBM (~1300 mA)
  - Vt1
    - Low Vt1 trigger voltage possible
    - Tunable using Spice simulator: RC filter calculations
  - Clamping voltage
    - Function of applied gate bias
    - Function of applied stress current



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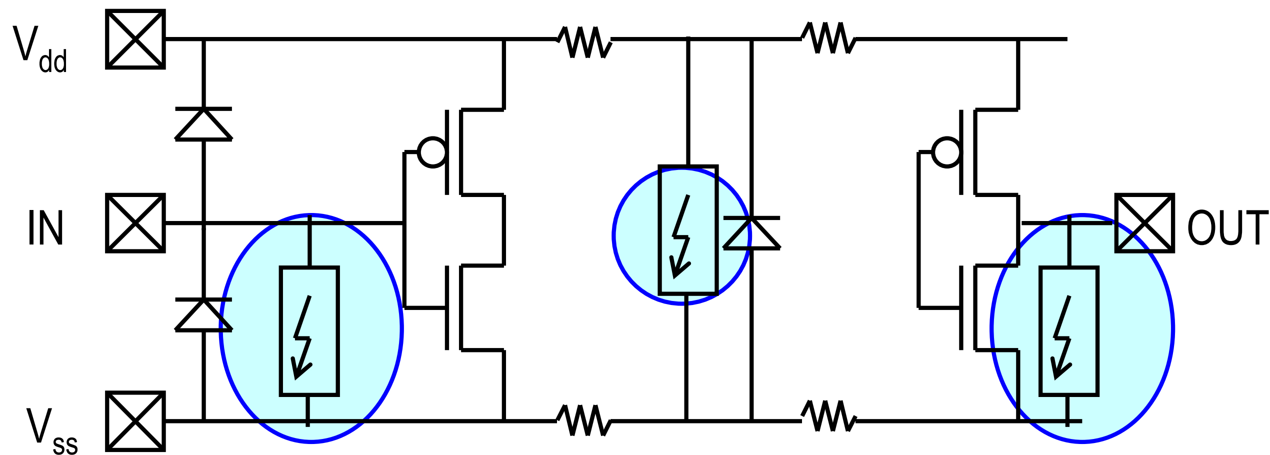
Basic ESD elements: SCR - use

- **Silicon Controlled Rectifier** is used for ESD protection
  - Power protection between Vdd and Vss
  - Local protection for input
  - Local, parallel protection for output drivers
  - **Used for many nodes, technologies**
  - **Difficult for system level requirements in HV technology**

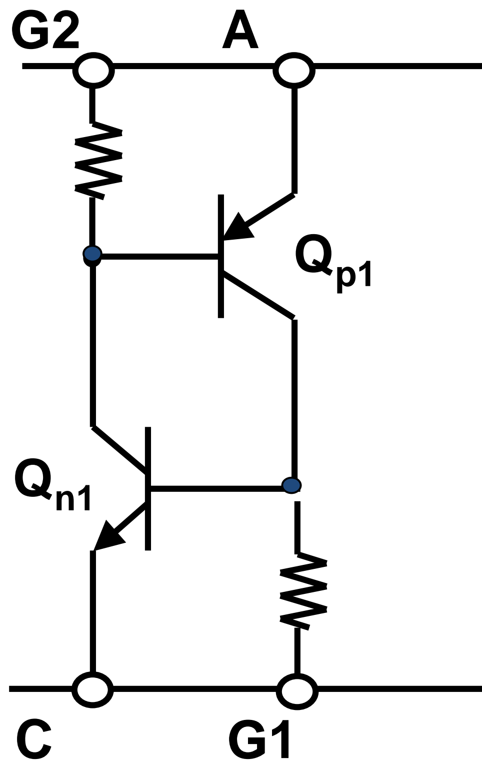


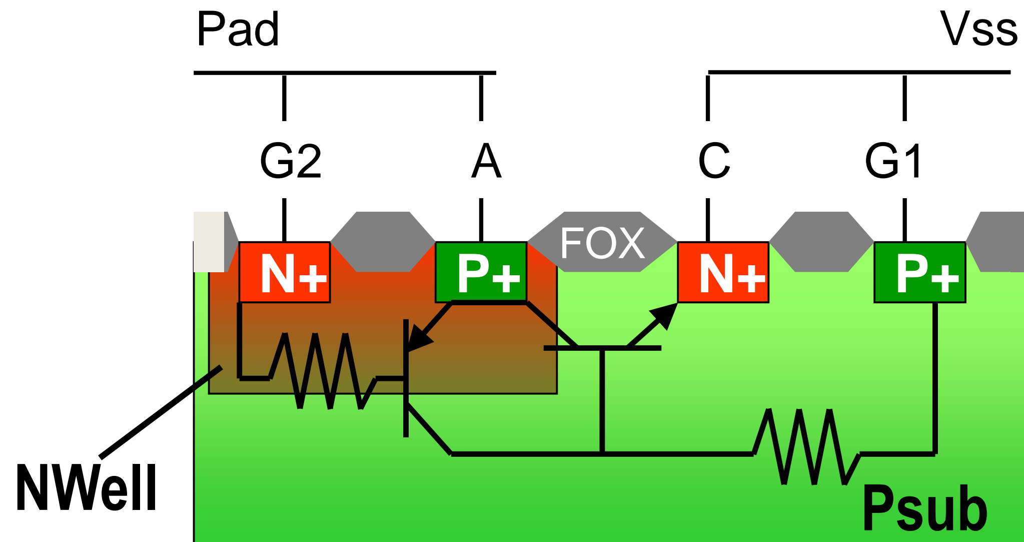
Silicon Controlled Rectifier ('SCR') or thyristor

- Different SCR versions
  - Basic Thyristor
    - Low holding voltage
    - Robust device
    - High trigger voltage: Nwell-Pwell breakdown
  - Internal triggering schemes
    - Reduced trigger voltage
    - Increased Anode Cathode spacing
      - Slow trigger speed
  - External triggering: Sarnoff TakeCharge®
    - Reduced, tunable trigger voltage
    - Small Anode Cathode spacing

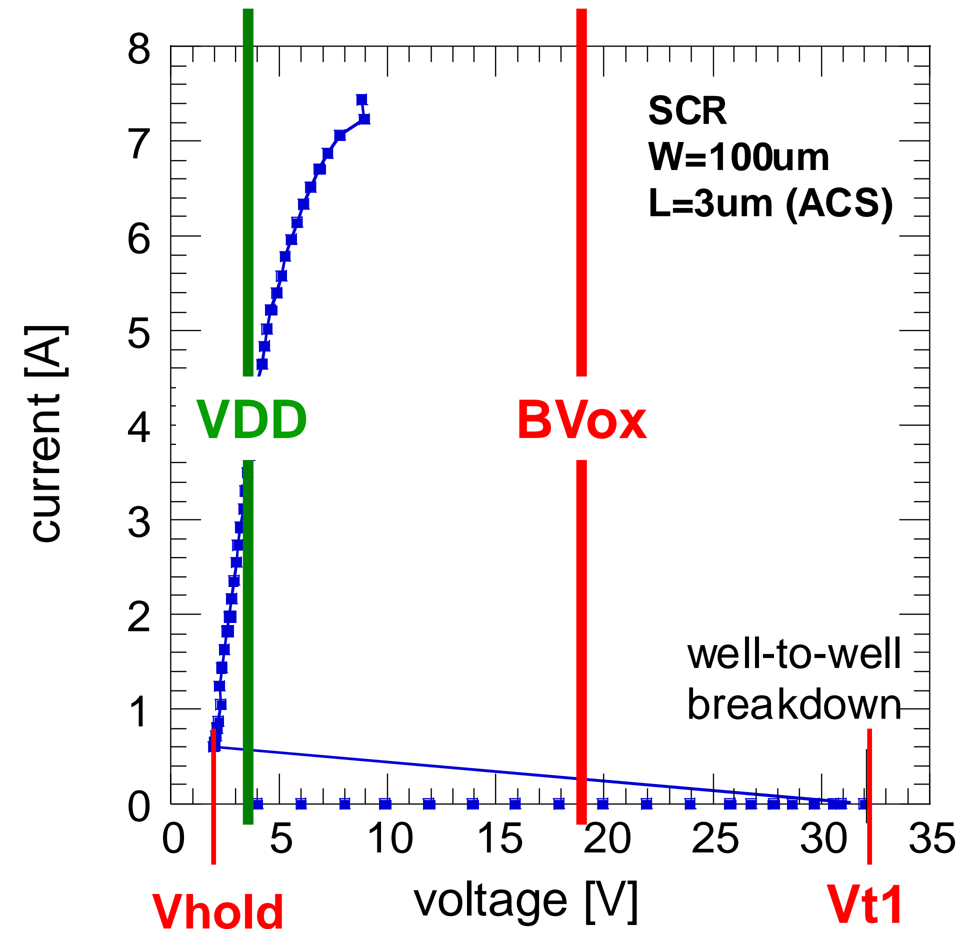
Protection Devices - SCR device

- Main principle:
  - Coupling of bipolar transistors creates regenerative action
  - Large current conduction possible





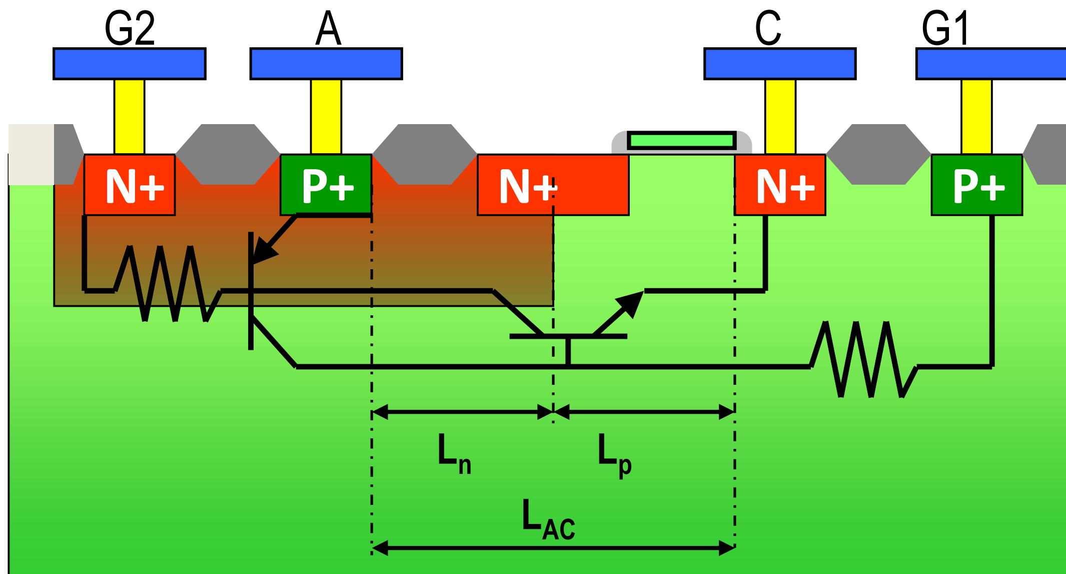
Basic SCR: High trigger voltage



- Basic SCR has a high trigger voltage
  - Nwell / Pwell breakdown voltage
  - Highly Process dependent
  - Vt1 > GOX breakdown

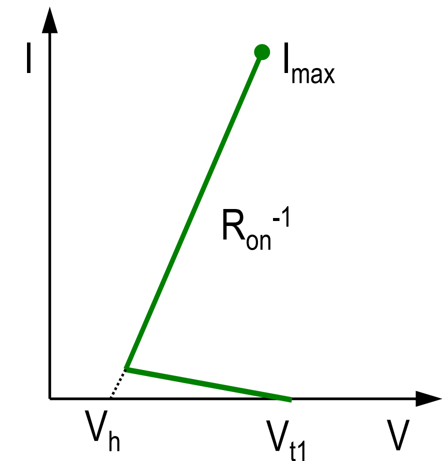
Trigger voltage reduction: internal trigger scheme

- LVTSCR (TI patent):
  - Integrated trigger element
  - Reduced trigger voltage: N+/Pwell breakdown
  - Large Anode Cathode spacing: LAC = Ln + Lp
    - Large bipolar (npn/pnp) base transit times
    - Not fast enough for advanced CMOS oxide protection



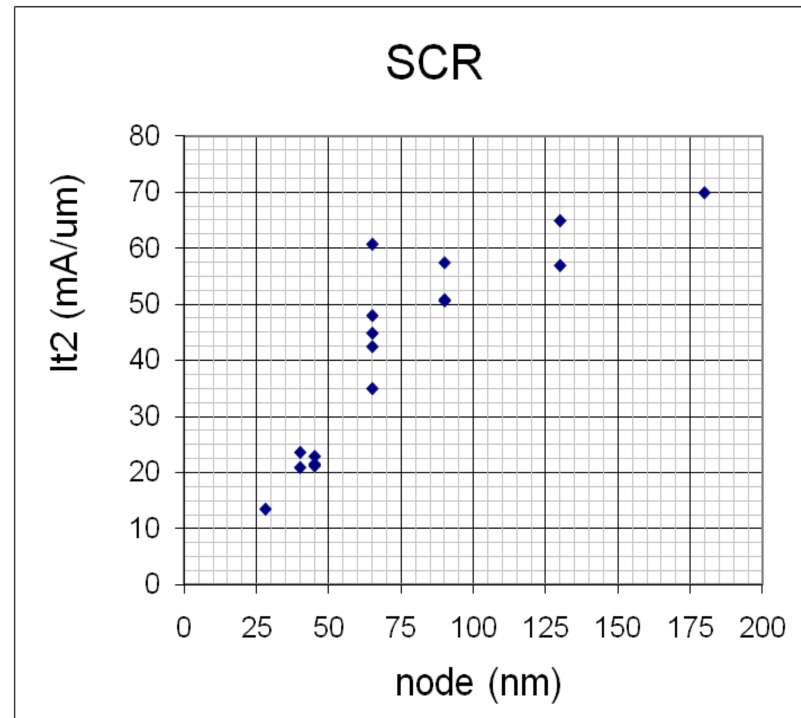
Basic ESD elements: SCR – Typical values

- Typical values for Silicon Controlled Rectifiers
  - Imax = ~ 50 mA/um
    - Example: 26um width required for 2kV HBM (~1300 mA)
  - Vt1
    - Basic SCR
      - Process dependent (doping levels)
      - Well-2-well breakdown, avalanching
      - Example: Vt1 = 40V for 14V process
    - LVTSCR
      - N+/PWell breakdown, avalanching
      - Example: Vt1 = 10V for 0.35um process
  - Vh
    - Function of the Anode Cathode distance ('LAC')
    - Typical value: Vh = 1.2V



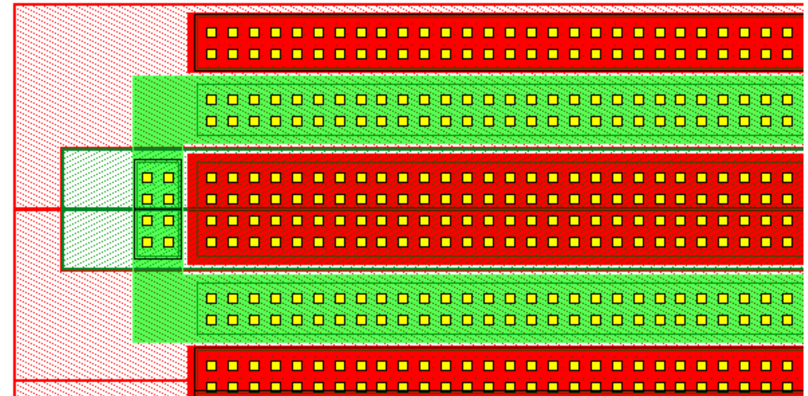
SCR

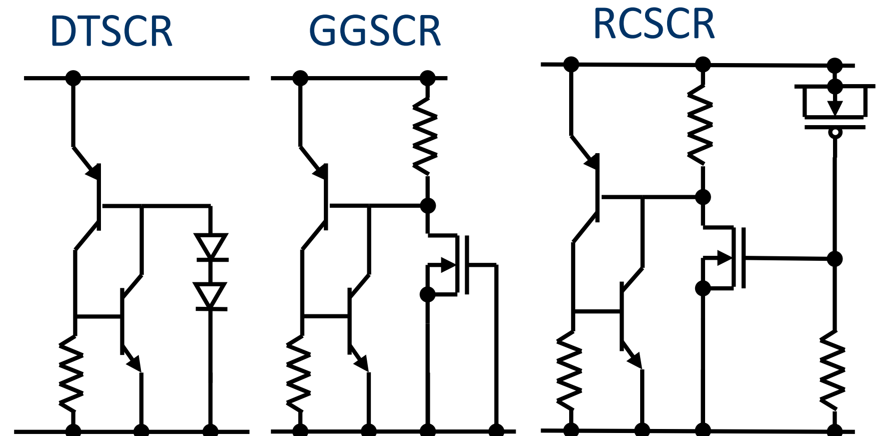
- Similar to diodes, the normalized performance / width is decreasing
  - Different trigger circuits were used for different technology nodes / power domains



TakeCharge® SCR – overview of parameters – device

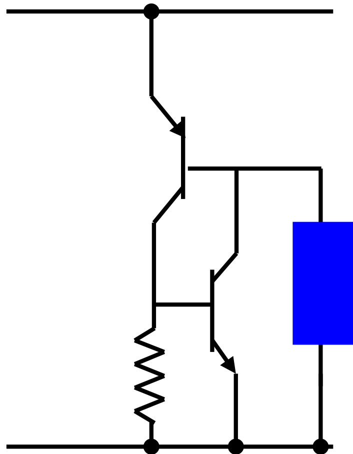
- TakeCharge SCR's for ESD protection
  - SCR Layout variations
    - Device width
    - Anode Cathode (A/C) distance
    - Contact rows on A/C
    - Nwell / Pwell structure
    - A/C Segmentation
  - Trigger element variations
    - Diodes, Bipolar, MOS,
  - ESD Detection variations
    - Static Voltage, Current level
    - Supply state detection
    - Dynamic Voltage, Current change

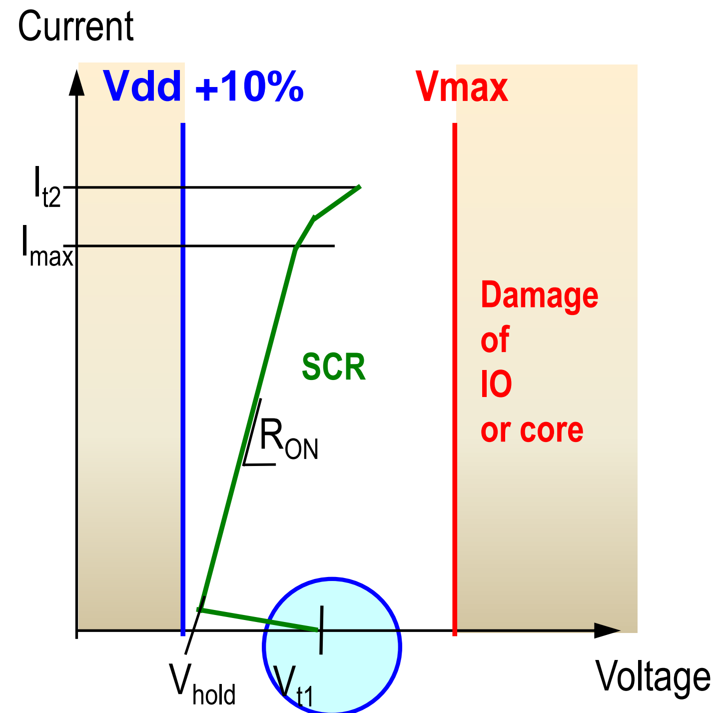




TakeCharge® SCR – summary

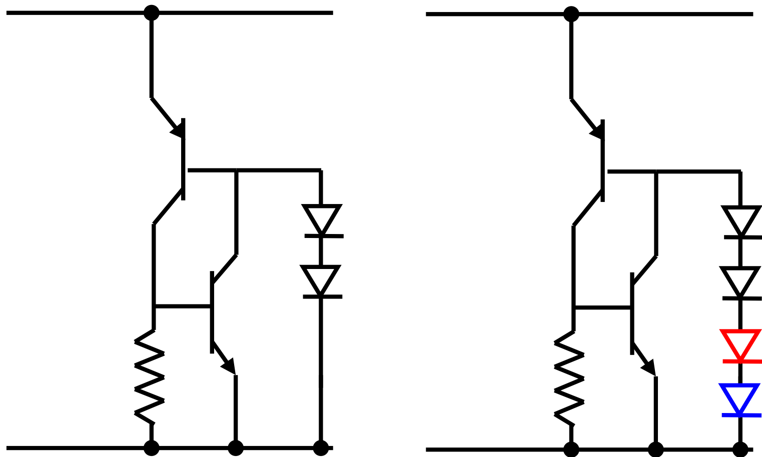
- Tunable trigger voltage Vt1
  - Determined by the **external trigger element**
  - Different options available

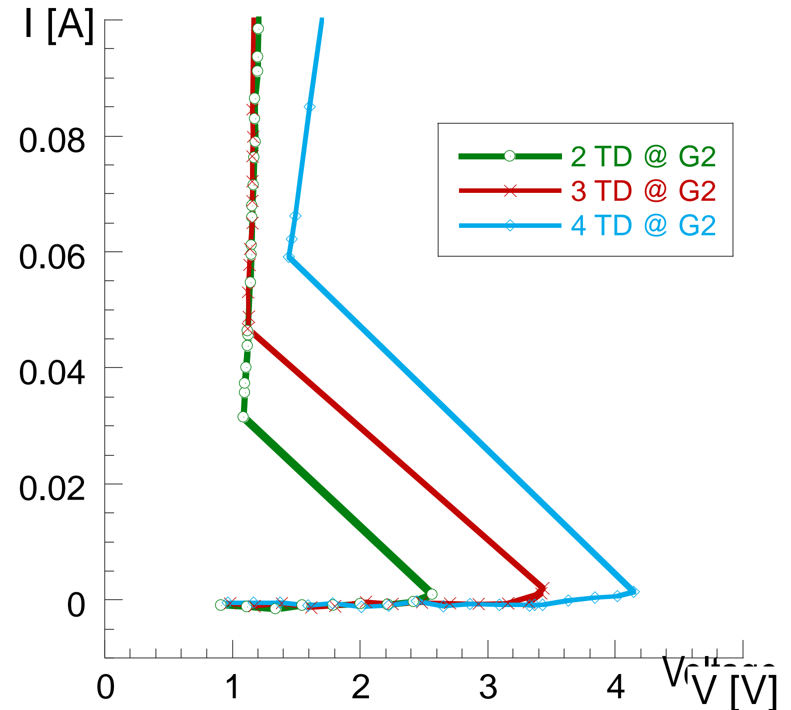




TakeCharge® SCR – Tunable trigger voltage Vt1

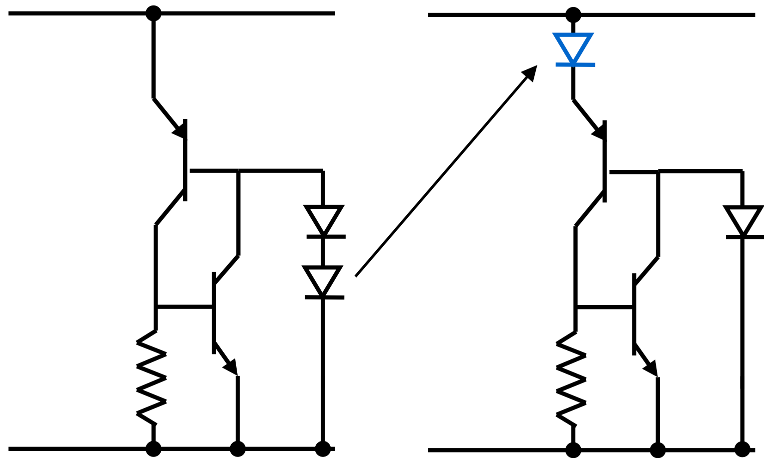
- SCR trigger variation:
  - Increased trigger voltage Vt1
  - Constant It2, Imax
  - Constant holding voltage Vhold

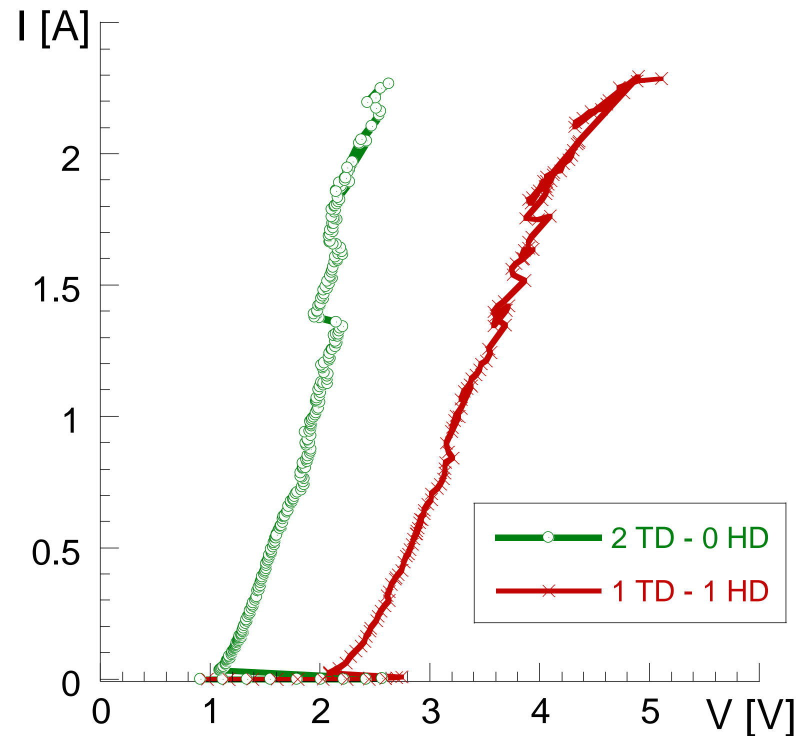




TakeCharge® SCR – Tunable holding voltage Vhold

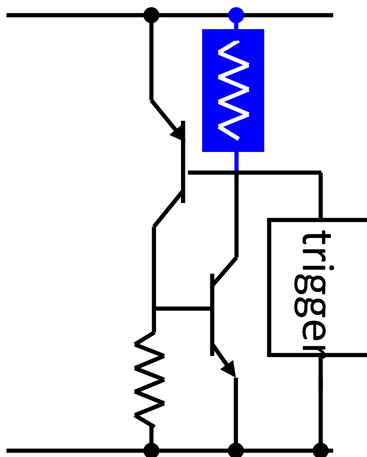
- SCR holding variation for Latch-up immunity
  - Determined by the **external series element**
  - Increased holding voltage Vhold
  - Constant trigger voltage Vt1



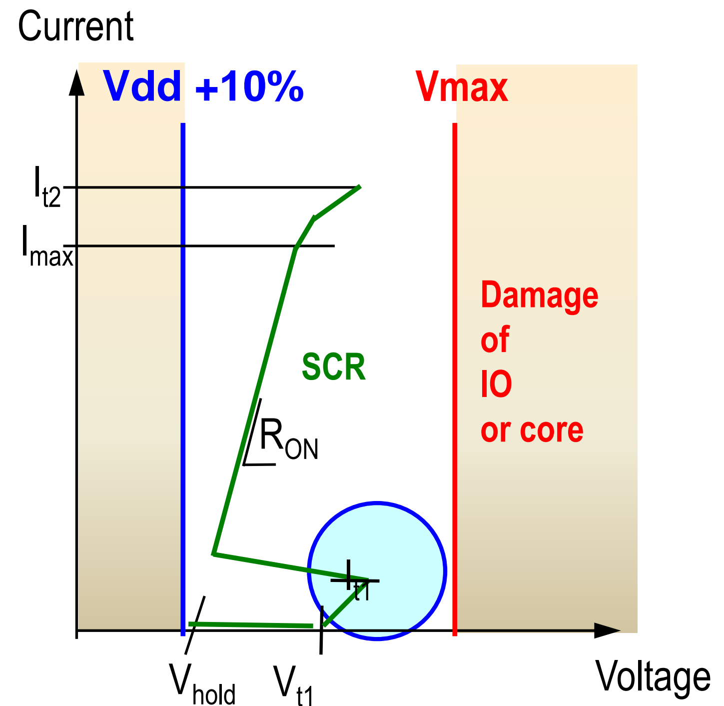


TakeCharge® SCR – Tunable trigger current It1

- Tunable trigger current It1
  - Determined by the **external resistance in trigger chain**
  - For improved latch-up immunity
    - Low R value → High It1

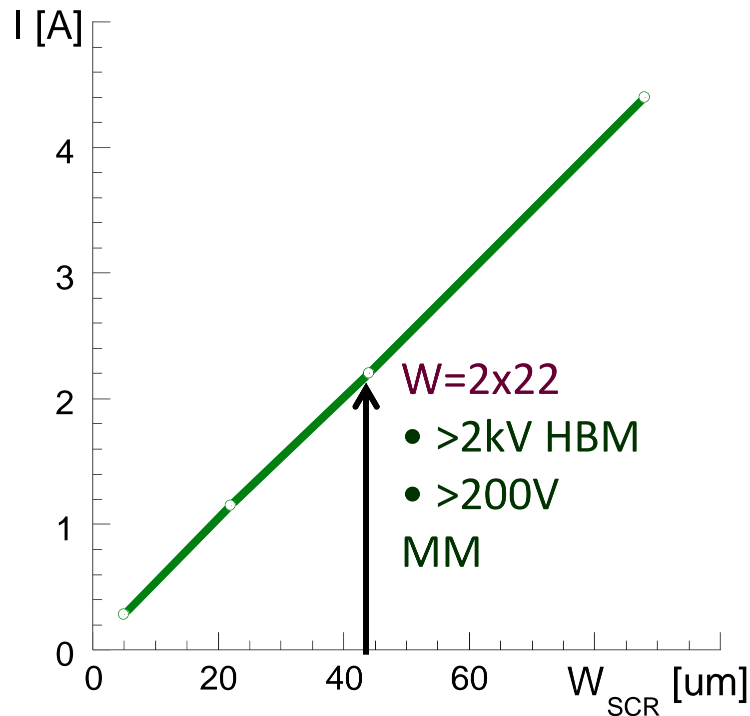


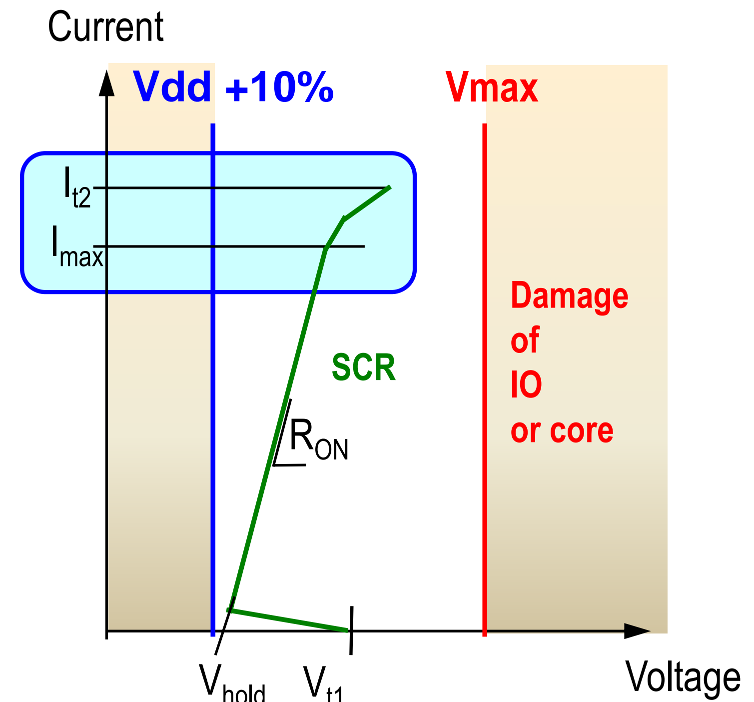
R_{iso} [ohm]	It1 [mA]
2	420
5	200
10	60



TakeCharge® SCR – Tunable failure current It2

- Tunable Failure current It2, Imax
  - Any ESD specification possible
  - Determined by the **SCR A/C width and # contact rows on A/C**
  - Example: DTSCR





Overview of ESD clamp devices

- Snapback Clamps
  - Avalanching junctions trigger clamp
    - Process tuning required: Avalanche voltage can shift
    - Trigger voltage can be high
    - Multiple clamps along power buses do not work well in parallel.
    - Examples: Snapback ggNMOS, LVTSCR, GG-SCR
  - Triggering without avalanche
    - Easy portable between process nodes
    - Trigger voltage tuning by
      - Diode strings, Active MOS elements, power-up state detection
    - Examples: DT-SCR, RC-SCR, ESD-on-SCR

Overview of ESD clamp devices

- Non-Snapback Clamps
  - Active MOSFET clamps
    - MOS action only
    - Very large width for low R clamp
    - Trigger circuit required
    - Examples: BIGFET approach
  - Diode Strings
    - String length sets stand-off voltage
    - Leakage at temperature can be a concern

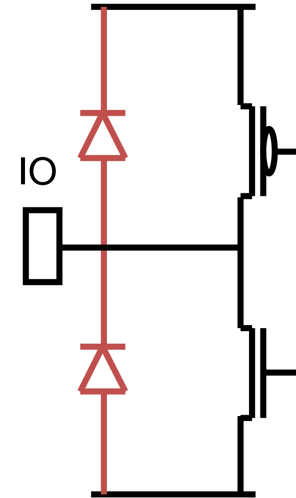
ESD protection devices and concepts

- Level 1: Devices: basic 'building blocks' or ESD devices?
  - Diodes
  - Snapback MOS / bipolar devices
  - Active mode MOS device
  - Silicon Controlled Rectifiers ('SCR')

- **Level 2: Protection concepts: arranging devices into protection circuits?**
  - **Dual diode**
  - **Self protective drivers**
  - **Full local protection**
  - **Secondary protection approach**

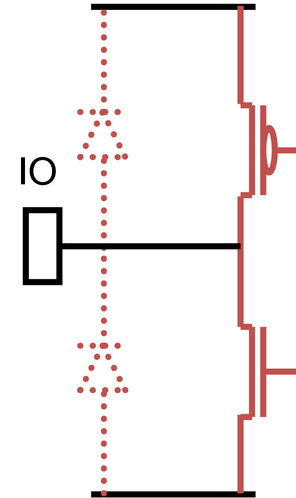
General protection concepts – dual diode

- Dual diode protection
  - Positive aspects
    - Area efficient protection
    - Low capacitance
    - Linear capacitance across voltage
  - Negative aspects
    - Bus resistance impacts ESD protection efficiency
    - Prohibits over voltage / under voltage tolerant interfaces



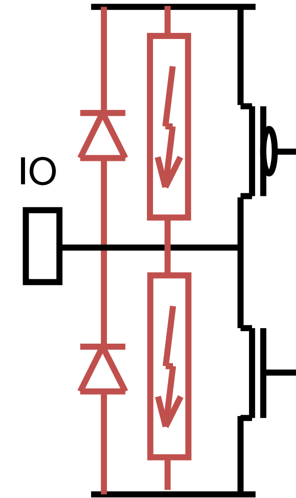
General protection concepts – Self protective

- Self protective output drivers
  - Positive aspects
    - Use ESD performance of the drivers
    - No diodes needed
  - Negative aspects
    - Large area
    - Large junction and gate capacitance
    - Non-uniform triggering issues



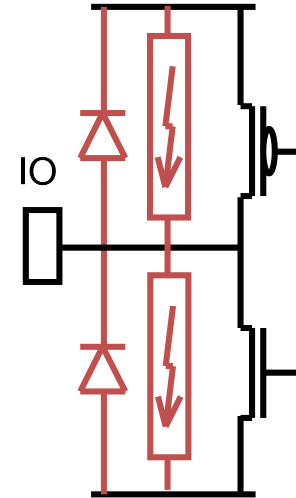
General protection concepts – Full local

- Full local protection
  - Positive aspects
    - Safe local clamping
    - Bus resistance is NOT critical
  - Negative aspects
    - Large area consumption (needed for every I/O pin)
    - Large capacitance



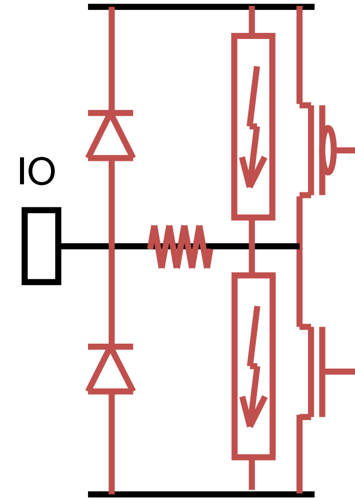
General protection concepts – Semi local

- Semi local protection
  - Positive aspects
    - Safe local clamping for NMOS driver/GOX
    - Bus resistance is LESS critical
  - Negative aspects
    - Large area consumption
    - Large capacitance
    - No solution for PMOS driver in IO case



General protection concepts – Secondary

- Secondary protection
  - Positive aspects
    - Use ESD performance of the drivers
    - Small local clamps
    - Safe local clamping
    - Bus resistance is LESS critical
  - Negative aspects
    - Isolation resistance
      influences normal operation (value: 50-500 Ohm)



Outline

- Introduction
- **ESD protection for advanced CMOS**
  - **Advanced CMOS nodes**
  - High voltages tolerant interfaces
  - Analog interfaces
  - Wireless interfaces
- ESD protection in high voltage, BCD
- ESD protection in SOI technology
- Summary, conclusions

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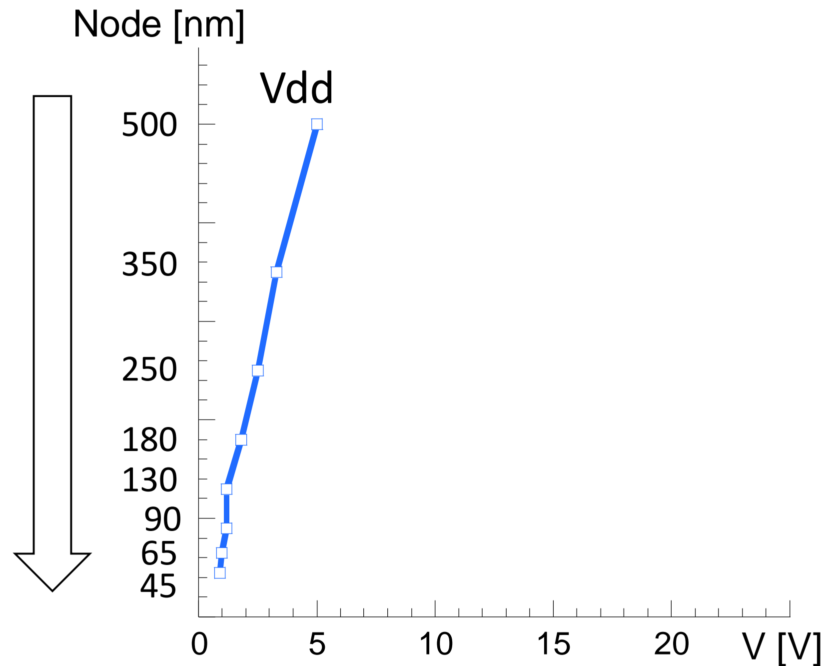
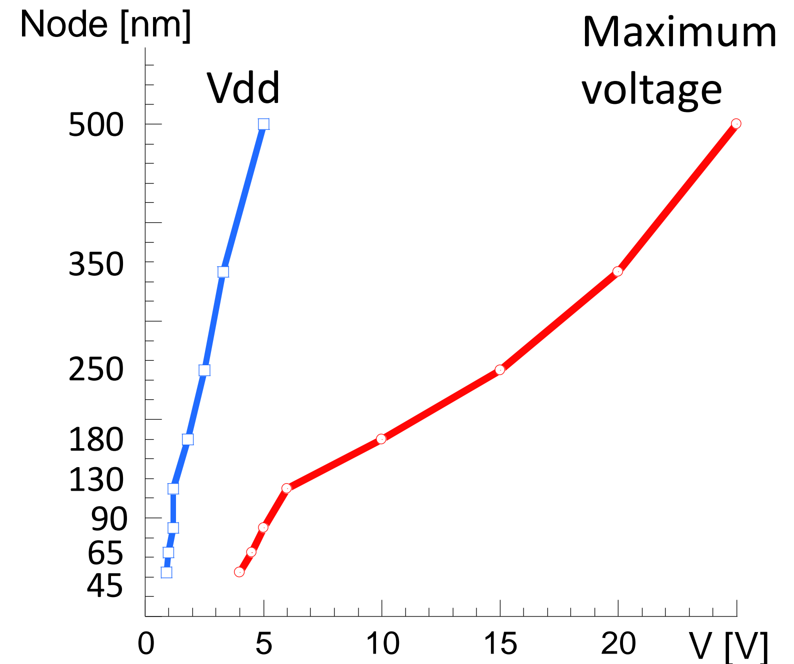
ESD Design Margin evaporates for advanced CMOS

- Decreasing solution space
  - Normal operation (VDD)
    - Slight decrease



ESD Design Margin evaporates for advanced CMOS

- Decreasing solution space
  - Normal operation (VDD)
    - Slight decrease
  - Maximum voltage decreases rapidly
    - Transient breakdown of gate oxides
    - Burn-out of output drivers
    - Core failure voltage



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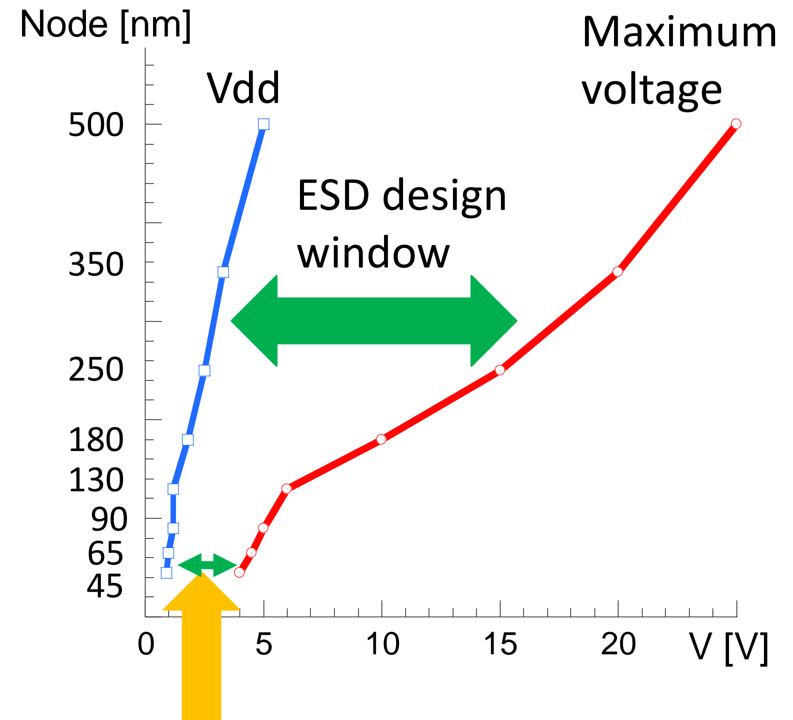
ESD Design Margin evaporates for advanced CMOS

- Decreasing solution space
  - Normal operation (VDD)
    - Slight decrease
  - Maximum voltage decreases rapidly
    - Transient breakdown of gate oxides
    - Burn-out of output drivers
    - Core failure voltage
  - Difference = ESD design window
    - **Rapid reduction of design margins**

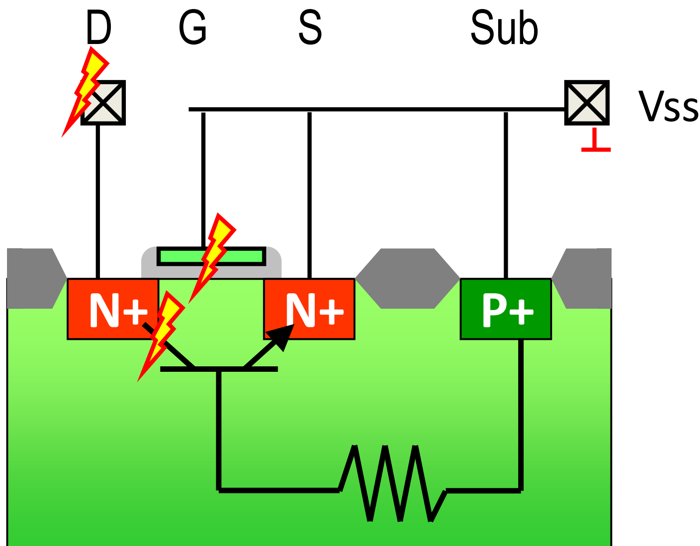


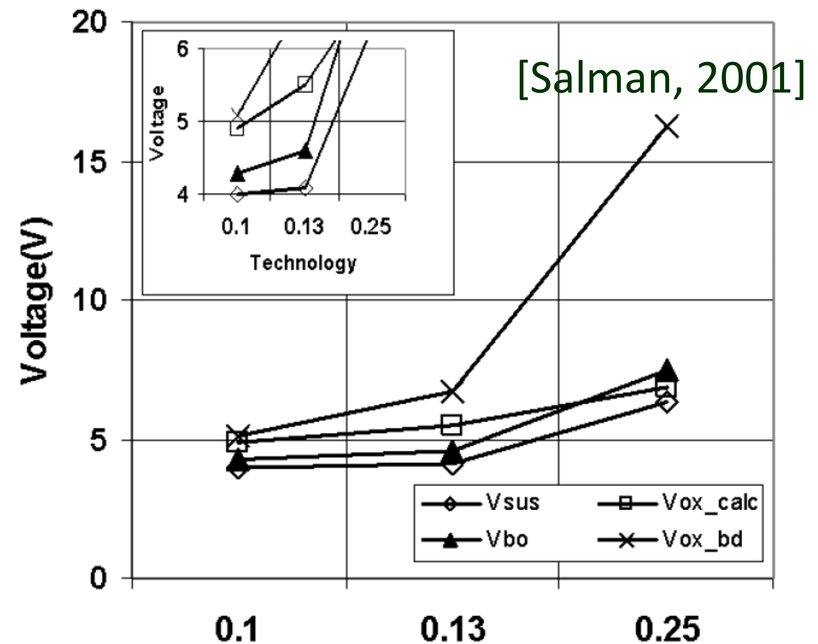
45nm/40nm:

ESD design space reduced to 3V!

Process scaling – ESD design window

- A. Salman (AMD), R. Gauthier (IBM), 2001
  - "Historically, the failure mode of the nMOS due is source-to-drain filamentation, ... **However, as the gate-oxide thickness shrinks, the ESD failure changes over to oxide breakdown**."





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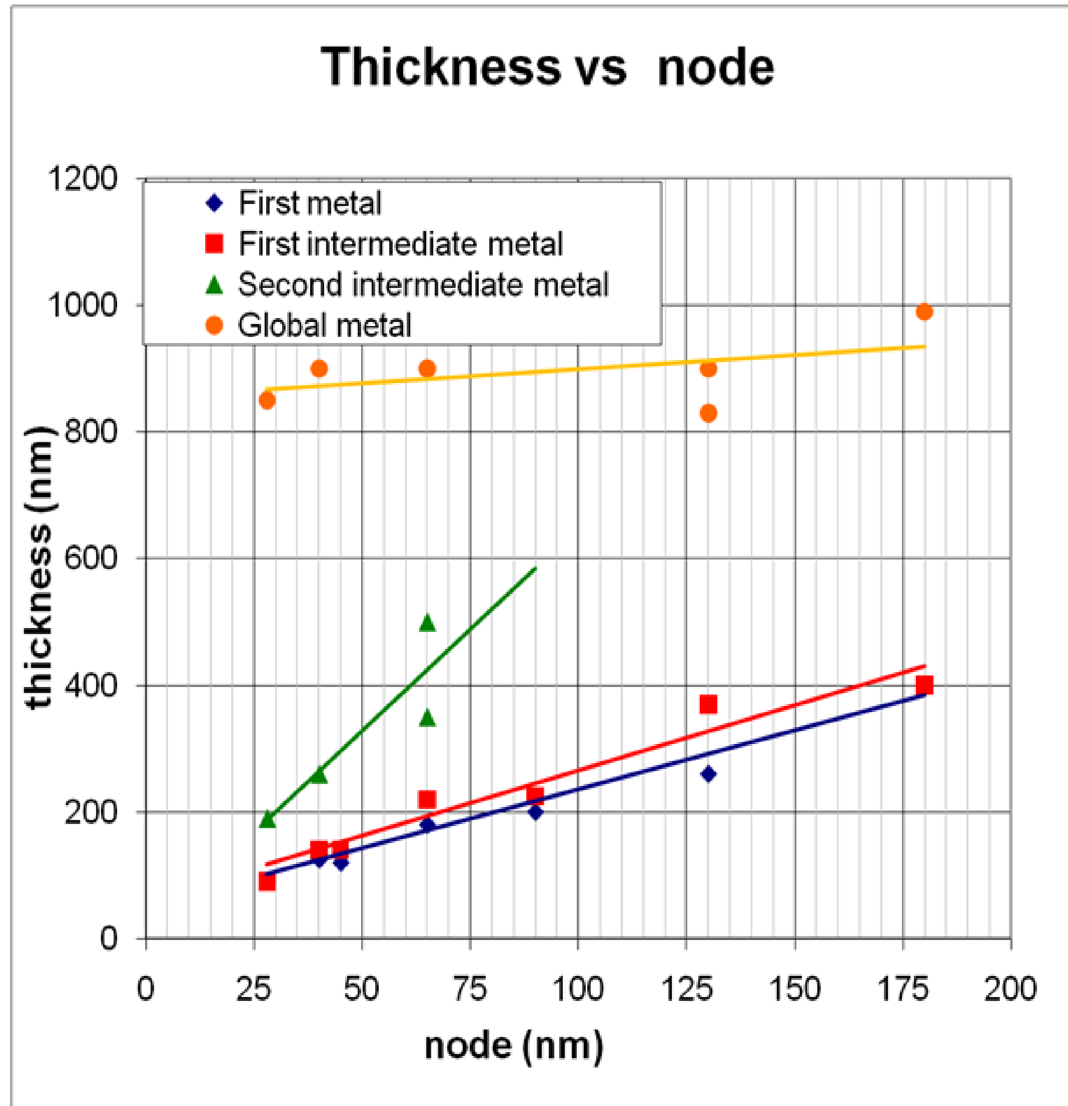
Metallization trends



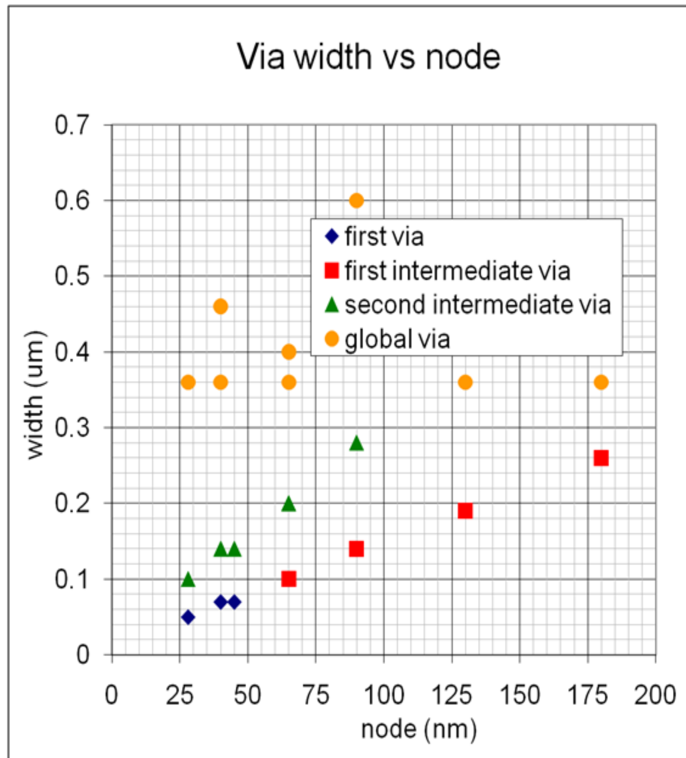
- 2 distinct groups of metallization
  - Local Metals
    - Decreased of thickness over 400 %
  - Top metal
    - Thickness hardly changed over the technologies

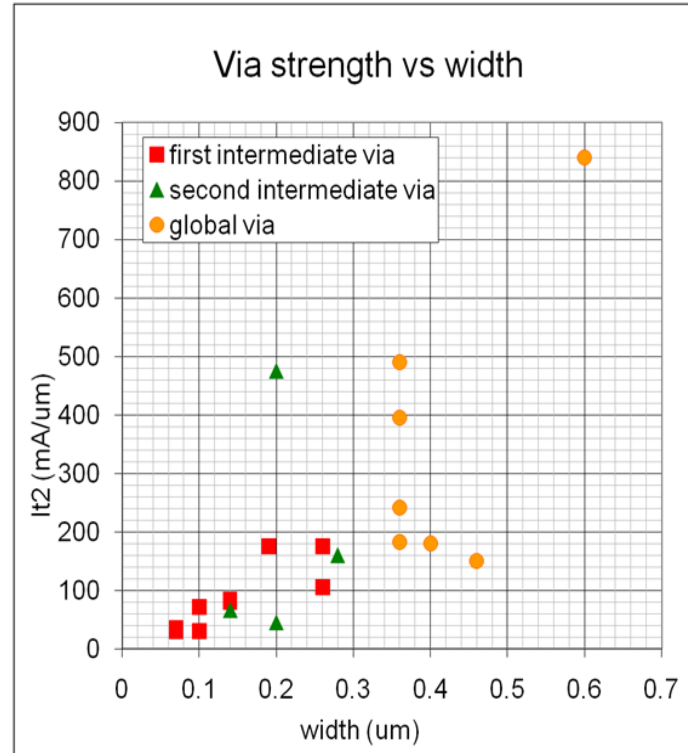
Metallization trends

- Metal strength depends on thickness
  - ESD robust power bus still possible
    - Top metal layers remain thick
  - Main difficulties in advanced technologies
    - Connections to the power bus
    - Internal connections inside the ESD clamp

Metallization trends: via and contact layers

- Similar trend is seen with the via layers
  - But less problematic since the via density is also increased





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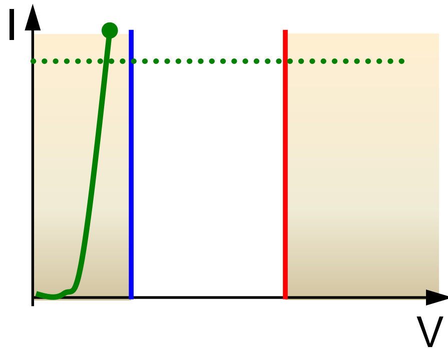
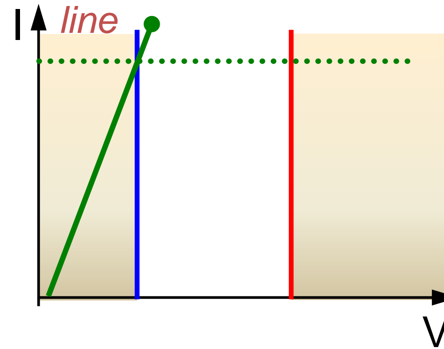
Impact on ESD protection strategy

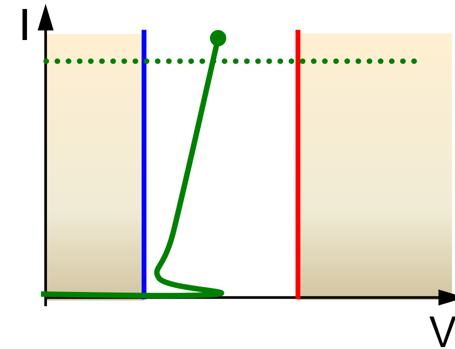
Diode

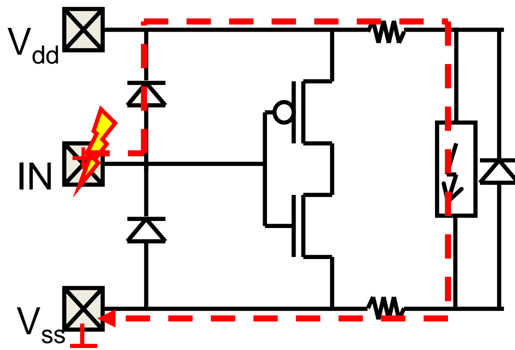


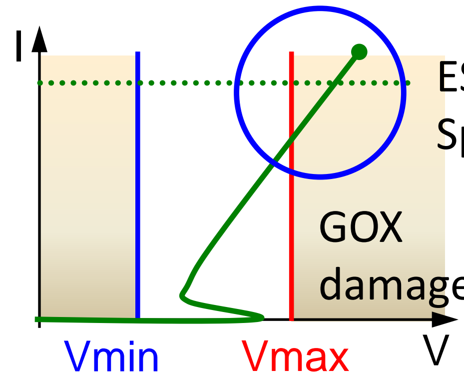
Resistance of Vdd, Vss bus line



Power Clamp







Robustness: OK

Effectiveness: NOT OK

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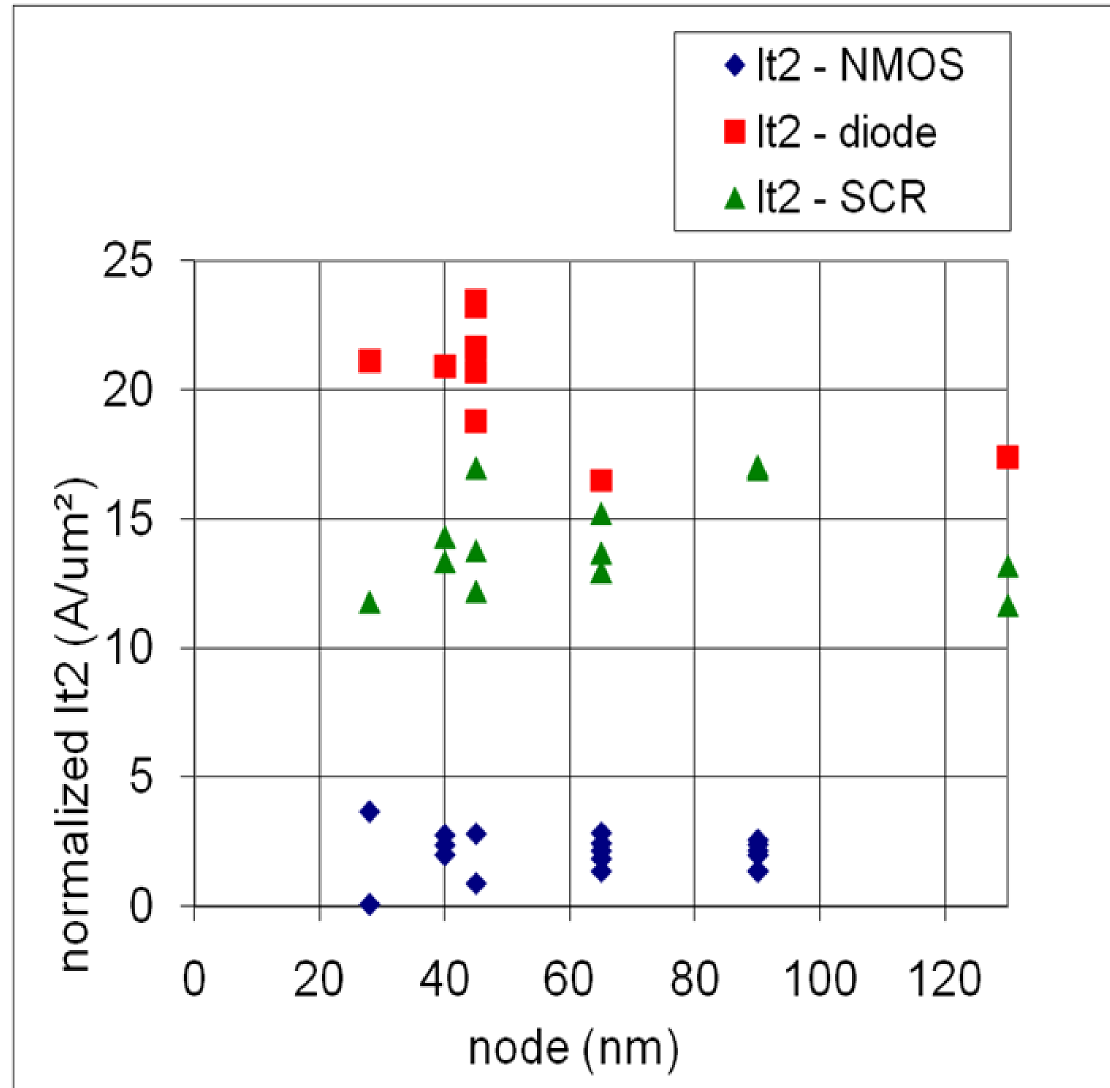
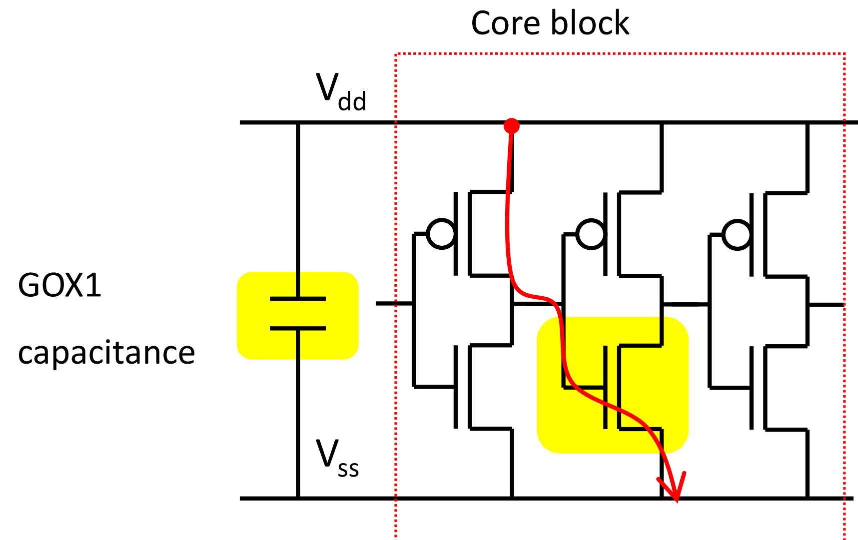
Impact on ESD Protection Strategy

- Normalized ESD performance
  - ESD performance per width is decreasing
  - Overall ESD performance per area stays the same
- If the ESD design is mainly determined by the failure current of the ESD clamp, the total ESD area does not increase for more advanced technologies.



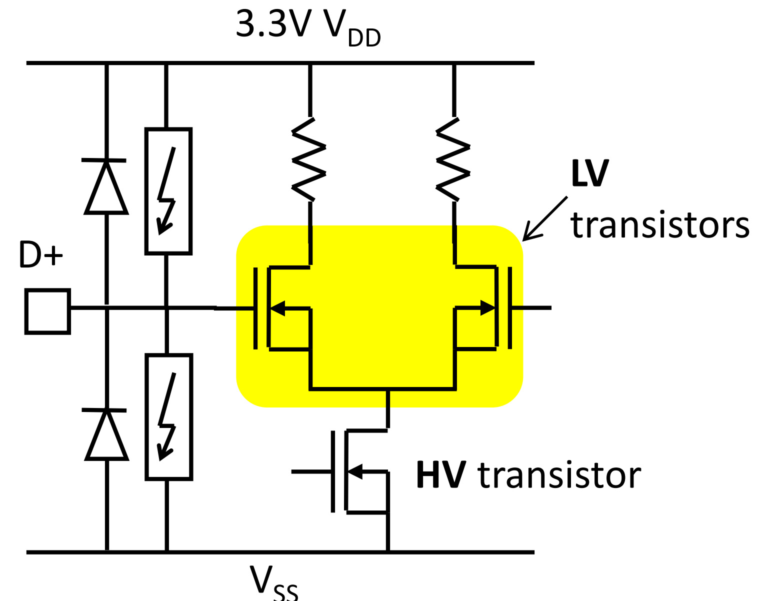
How about your ASIC circuits?

- Dangerous situations (1/4)
  - Cause: Include on-chip decoupling capacitors
    - Stabilize Vdd supply potential
    - Reduce board level components: BOM
    - Designers use GOX1 gate capacitance: highest Cap/area
  - Problem:
    - LV Core breakdown determined by sensitive thin gate oxide
    - Reduced ESD design margin
  - Solution:
    - Low voltage triggered power clamp



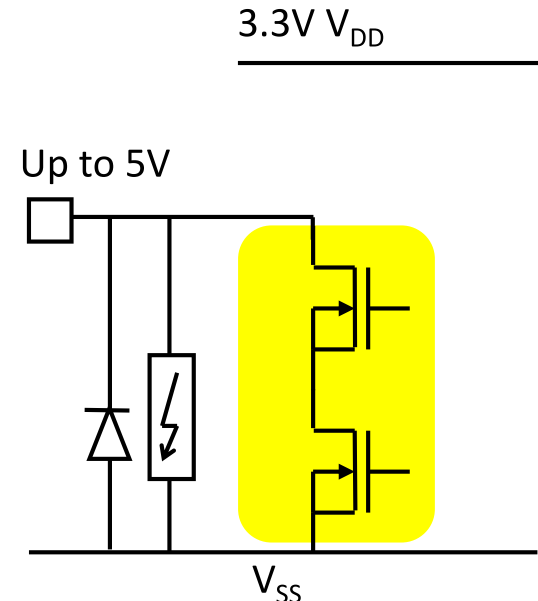
How about your ASIC circuits?

- Dangerous situations (2/4)
  - Cause:
    - Analog tricks to improve circuit speed
    - Include core transistors in 3.3V domain
    - Designers use GOX1 transistor for speed reasons
    - Designers do not use ESD foundry rules
  - Problem:
    - HV Core breakdown determined by sensitive thin gate transistor
    - Reduced ESD design margin
  - Solution:
    - Low voltage triggered power clamp for High Voltage domain



How about your ASIC circuits?

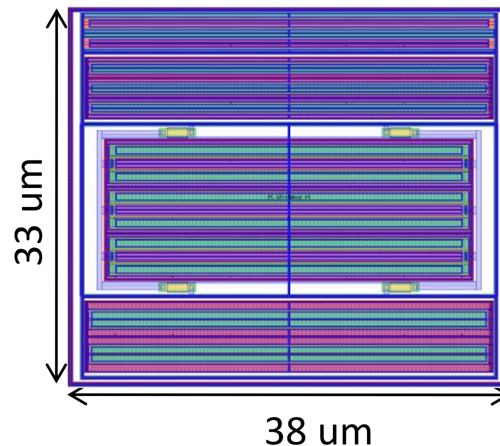
- Dangerous situations (3/4)
  - Cause:
    - Cascode configurations
    - Increase signal voltage tolerance (5V tolerant)
    - Designers do not use ESD foundry rules
  - Problem:
    - Unballasted cascode design ESD sensitive
    - Reduced ESD design margin
  - Solution:
    - Improved cascode layout
    - Local (IO) protection approach

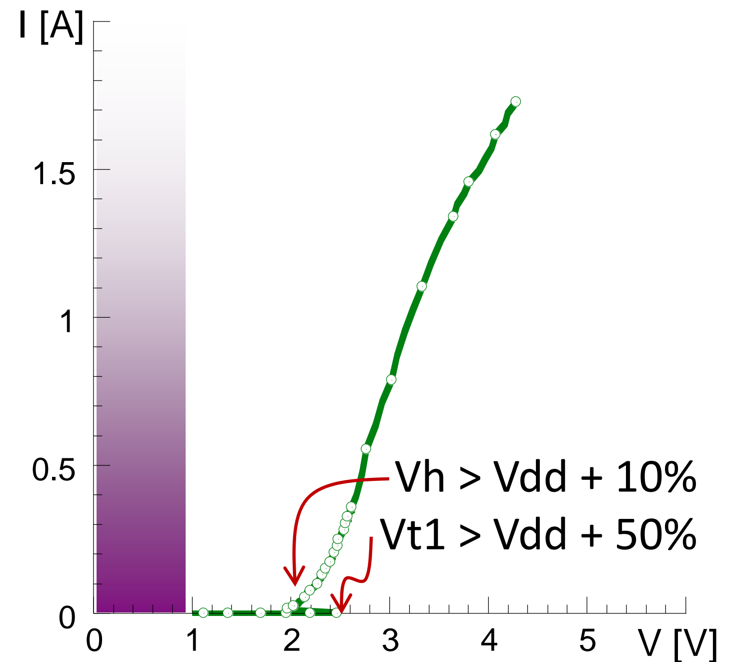


How about your ASIC circuits?

- Issues 1-3
  - Reduced ESD design margins
  - Example solution
    - 40nm CMOS – 0.9V domain
    - 3.6kV HBM
    - 245V MM
    - < 100pA leakage

40nm 0.9V power clamp example

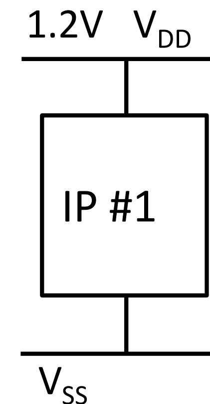




SoC's add another level of complexity

- SoC's main ESD problem?
  - IP block 1: Within specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven

IP#1 alone
>2kV HBM,
>500V CDM



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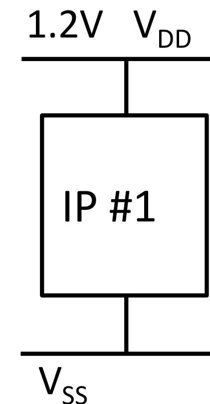
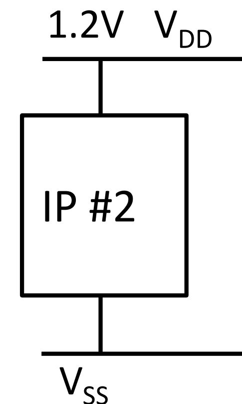
SoC's add another level of complexity

- SoC's main ESD problem?
  - IP block 1: Within specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven
  - IP block 2: Above specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven

IP#1 alone
>2kV HBM,
>500V CDM

IP#2 alone
>4kV HBM,
>1000V CDM





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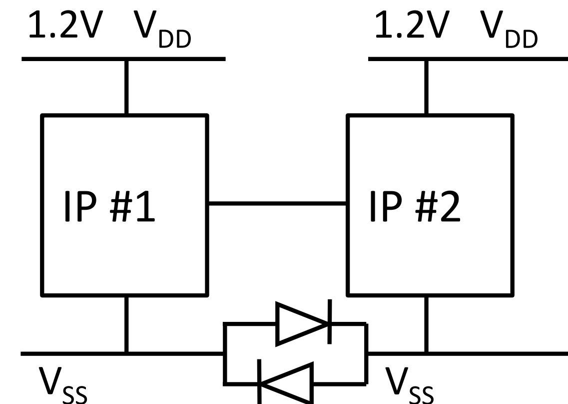
SoC's add another level of complexity

- SoC's main ESD problem?
  - IP block 1: Within specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven
  - IP block 2: Above specs
    - Fully qualified for ESD protection
    - Silicon proven, product proven
  - Wired together in SoC: Below spec
    - Functionality: OK
    - ESD qualification: **below spec!**
    - **Which IP provider is responsible?**

Full product
<1kV HBM,
<100V CDM

IP#1 alone
>2kV HBM,
>500V CDM

IP#2 alone
>4kV HBM,
>1000V CDM



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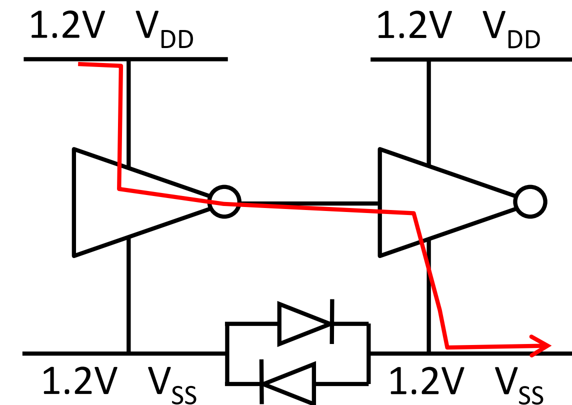
How about your ASIC circuits?

- Dangerous situations (4/4)
  - Cause:
    - Multiple functional core blocks – separately biased
    - Multiple voltage domains (Digital, Analog, IO, ...)
    - Multiple IP blocks from various vendors
  - Problem:
    - Unprotected internal / on-chip communication lines
  - Solution:
    - Ground to ground
    - Improved cascode layout
    - Local (IO) protection approach



Conclusions

- Growing difficulty for ESD protection
  - Advanced CMOS
  - Complex System-on-Chip designs
- Public solutions
  - Exploding silicon cost, increased risk (Industry group)
  - IO based protection not suffucient
  - Core interface circuits need specific care
- **Solutions available**
  - Treat on-chip interfaces as external interfaces for ESD
  - Include protection clamps at sensitive receiver

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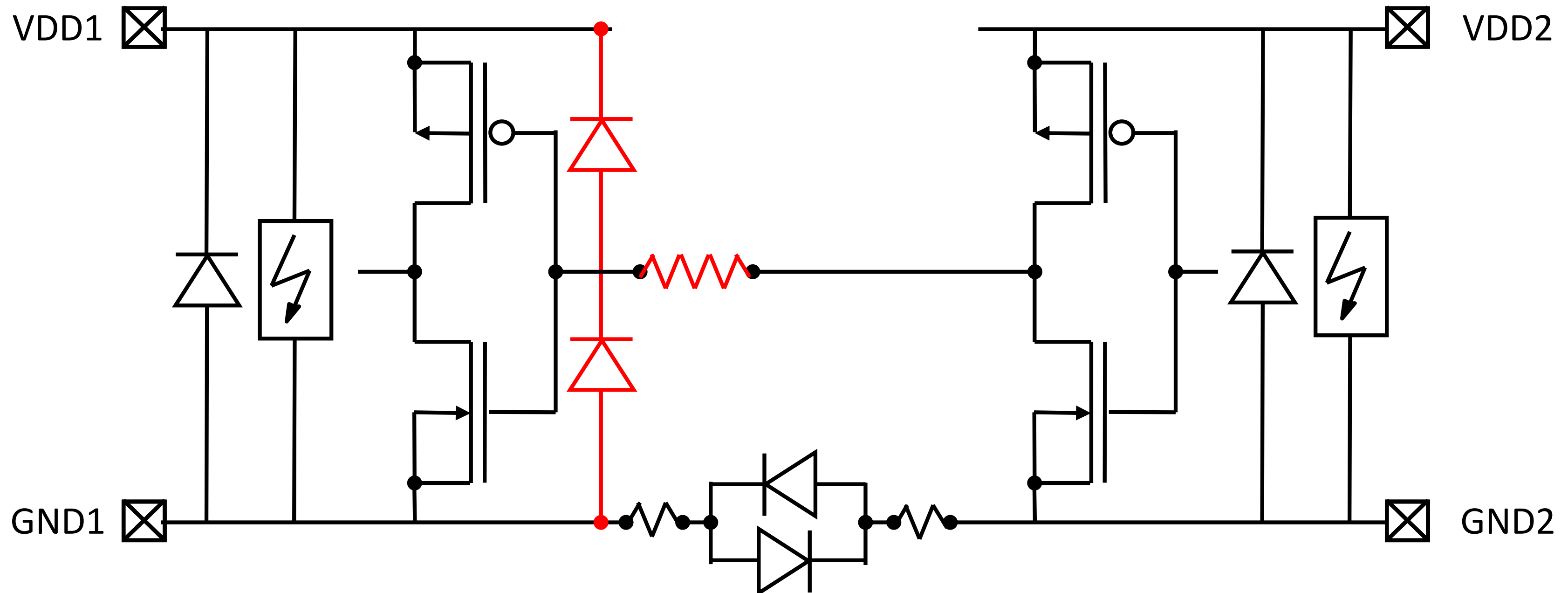
Simple solution to core failures?

- L. Avery (Sarnoff patent), 1996 – **Rubber band** technique
  - Multi domain core protection
  - Isolation resistance to limit the current
  - Local gate protection for most sensitive gates



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Outline

- Introduction
- **ESD protection for advanced CMOS**
  - Advanced CMOS nodes
  - **High voltages tolerant interfaces**
  - Analog interfaces
  - Wireless interfaces
- ESD protection in high voltage, BCD
- ESD protection in SOI technology
- Summary, conclusions

SOFICS
SOLUTIONS FOR ICs

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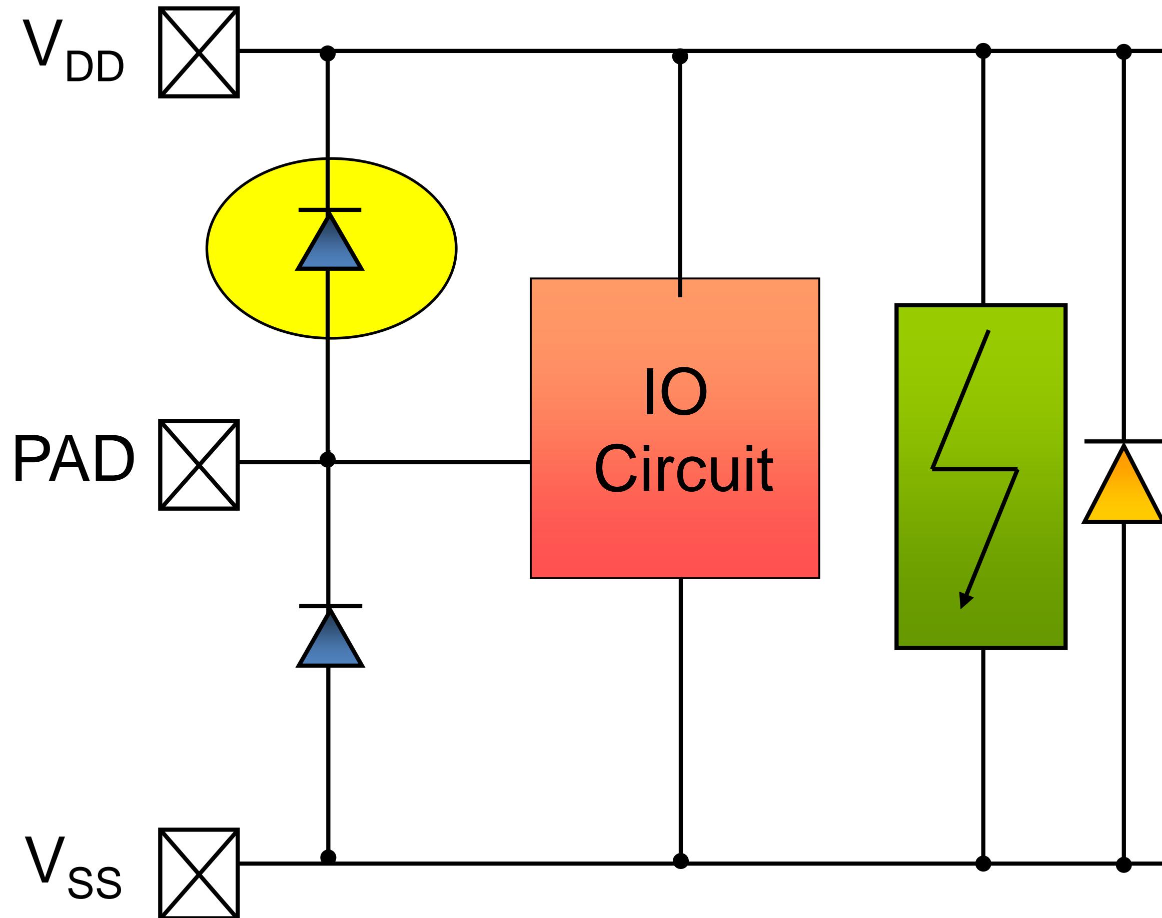
A simple diode... creating so many problems



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Example: Signal voltage above VDD

- Signal voltage above VDD level
  - Various reasons
  - Diode from PAD to VDD not tolerated

Vdd potential

Signal potential

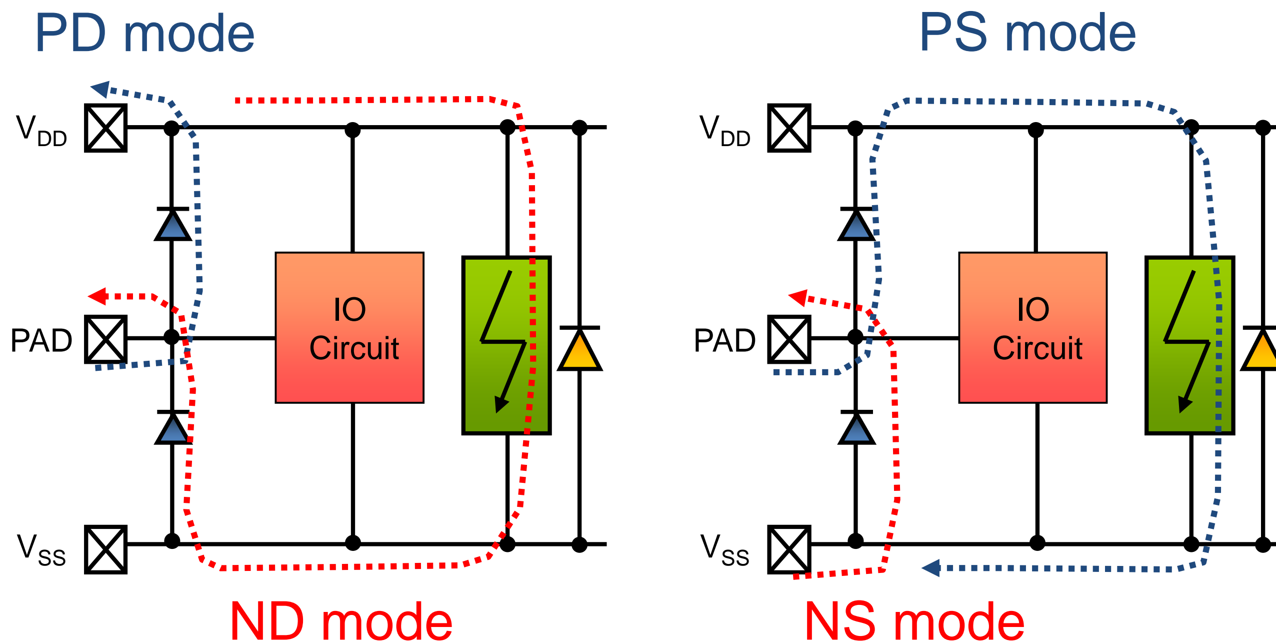
V_{dd}

IN

V_{ss}

Introduction: diode based IO ESD protection

- Dual diode approach
  - Most used IO ESD protection concept
  - Protection for PD, PS, ND, NS modes



‘Diode up’ influences functional performance

- Diode up reduces IC performance
  - Remove ‘diode up’
    - Stress cases PD, PS need to be covered differently

PD mode ??

V_{DD}

PAD

IO Circuit

V_{SS}

PS mode ??

V_{DD}

PAD

IO Circuit

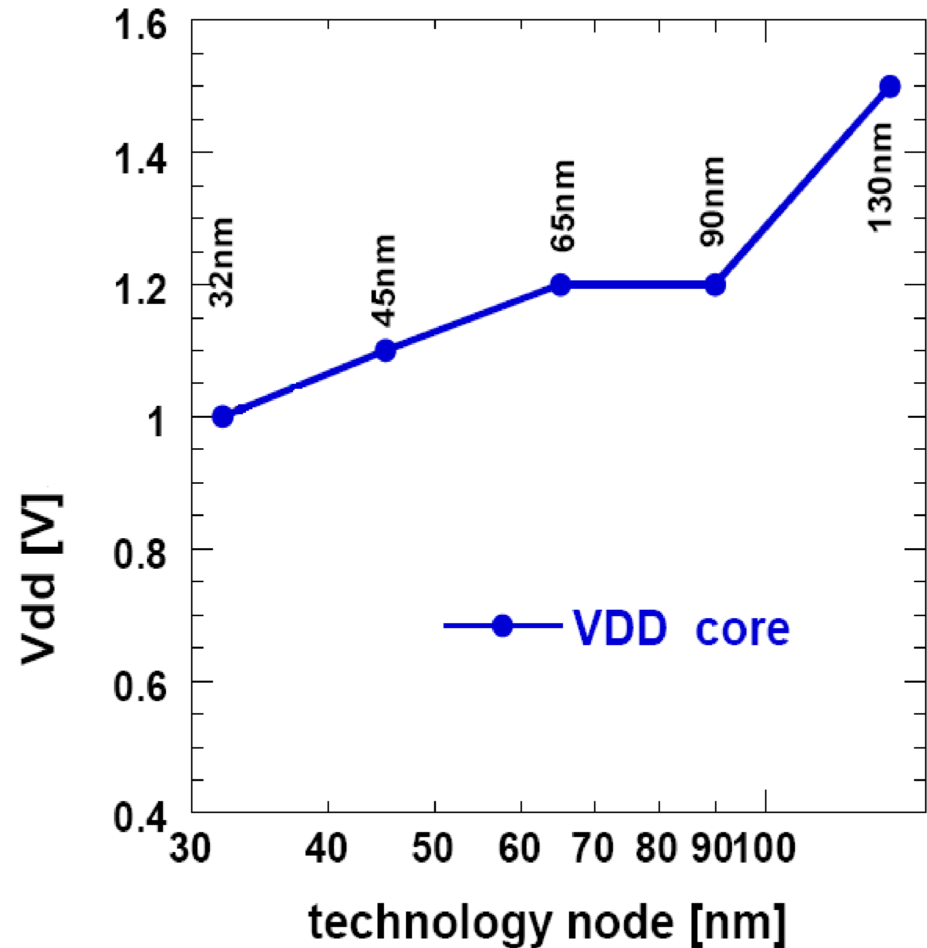
V_{SS}

Outline about overvoltage tolerant

- Introduction
- Diode up problems
  - Voltage level differences between ICs
  - Shared communication line
  - High speed interface
  - Hot swap
  - Backdrive protection
  - Inductive loads
  - Protection of sensitive transistors
  - ...
- Solution concepts
- Solution examples
- Conclusion

IC technology trends – V_{DD} levels reducing

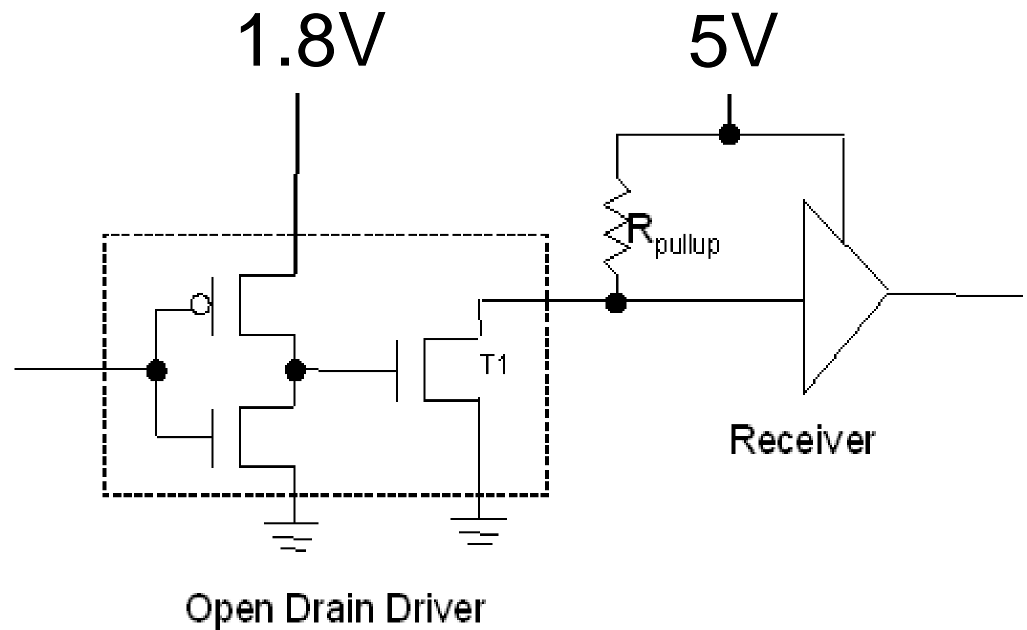
- Technology scaling
  - Reduction of core supply voltage continues
    - 1.5V at 130nm
    - 1.0V at 32nm
    - 0.85V at 28nm
  - Pace defined by ITRS
- What about IO voltage?



Ref: IEW 2010 – Christian Russ, Infineon

Typical solution: Open drain outputs

- Open drain driver
  - Translate low voltage to higher voltage
  - Simple pull-up resistance concept



Ref: EETimes Prasad Dhond, Texas Instruments

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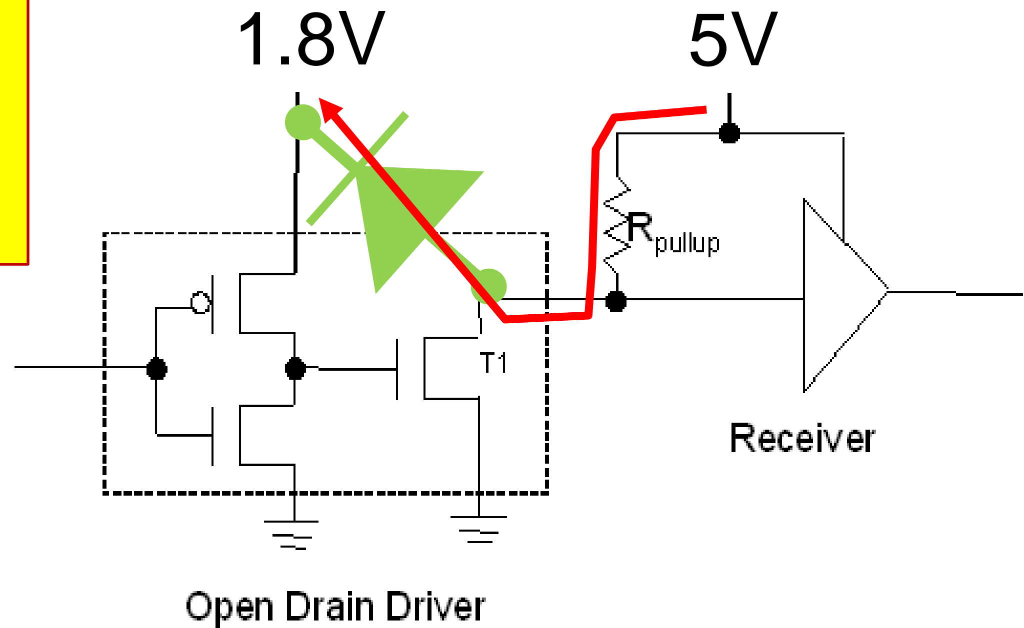
Open drain output: ESD protection issue

- Open drain driver: Diode to V_{DD} not tolerated
  - NMOS T1 OFF
  - 1.8V level influenced by 5V supply

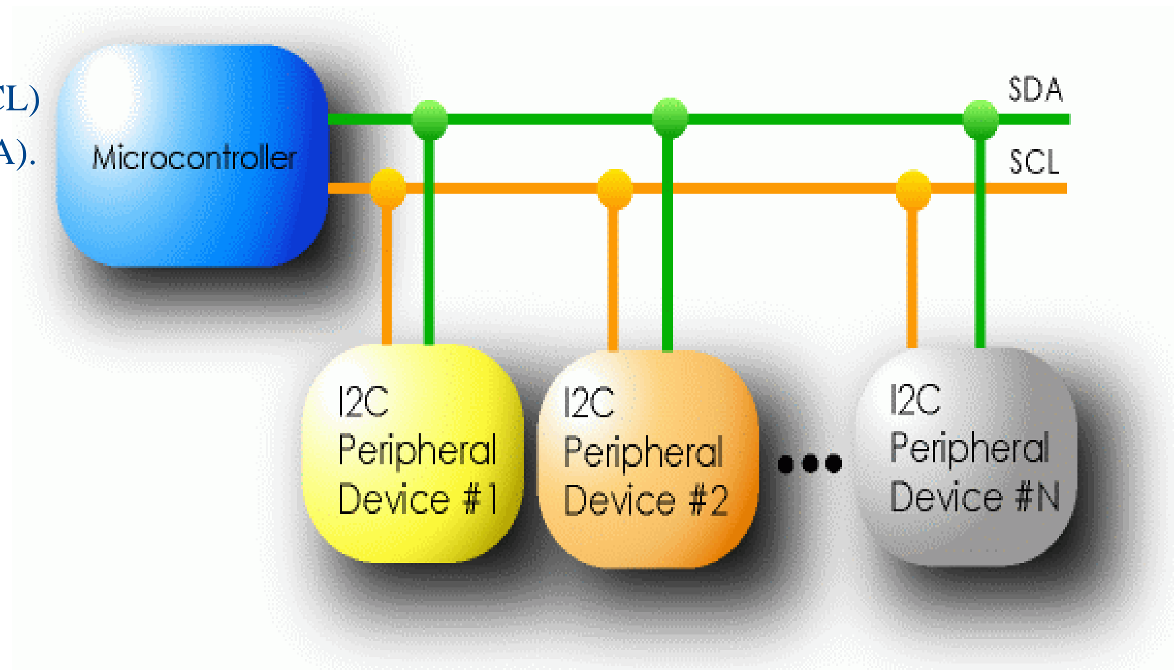
Voltage differences

Another ESD protection concept required



Shared communication lines

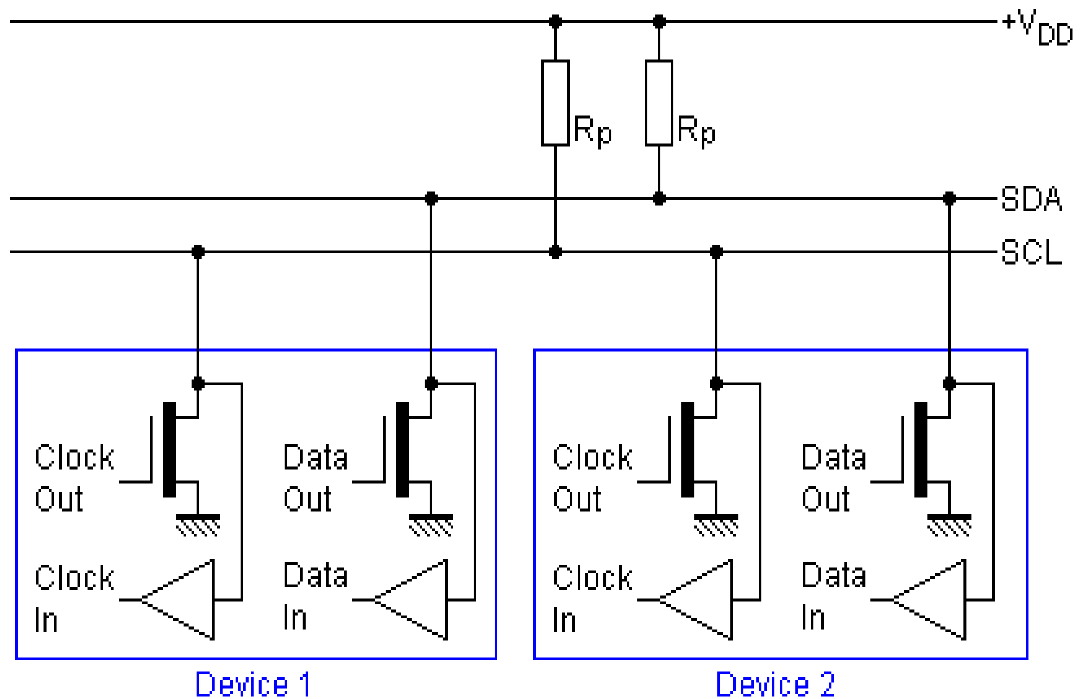
- Several ICs communicate through 2 shared lines
  - Example I²C bus
    - 2-wire,
    - Half-duplex
    - Serial bus
    - Two I²C signals
      - serial clock (SCL)
      - serial data (SDA).
    - Bidirectional lines



Ref: Volker Soffel, MCPros corporation

Shared communication lines: open drain IO

- Shared communication line – simplified schematic
  - Pull-up resistance to V_{DD}
  - Open drain NMOS
  - Different V_{DD} voltage possible but not necessary



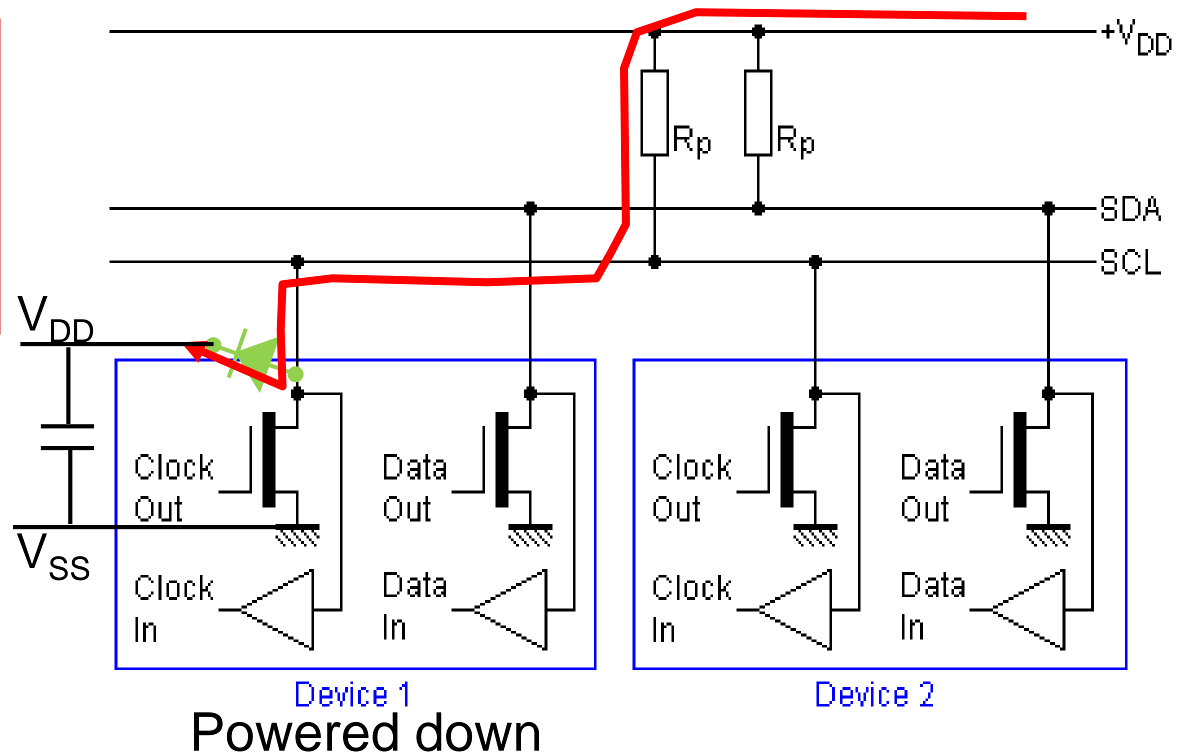
Ref: Wikipedia

Communication line: ESD protection issue

- Shared communication: Diode to V_{DD} not tolerated
  - E.g. powered down device 1

Shared buslines

Another ESD protection concept required



HDMI: Digital video system

- Example: HDMI connection
  - LCD TV receiver
  - DVD player
  - HDMI connection
    - TMDS approach

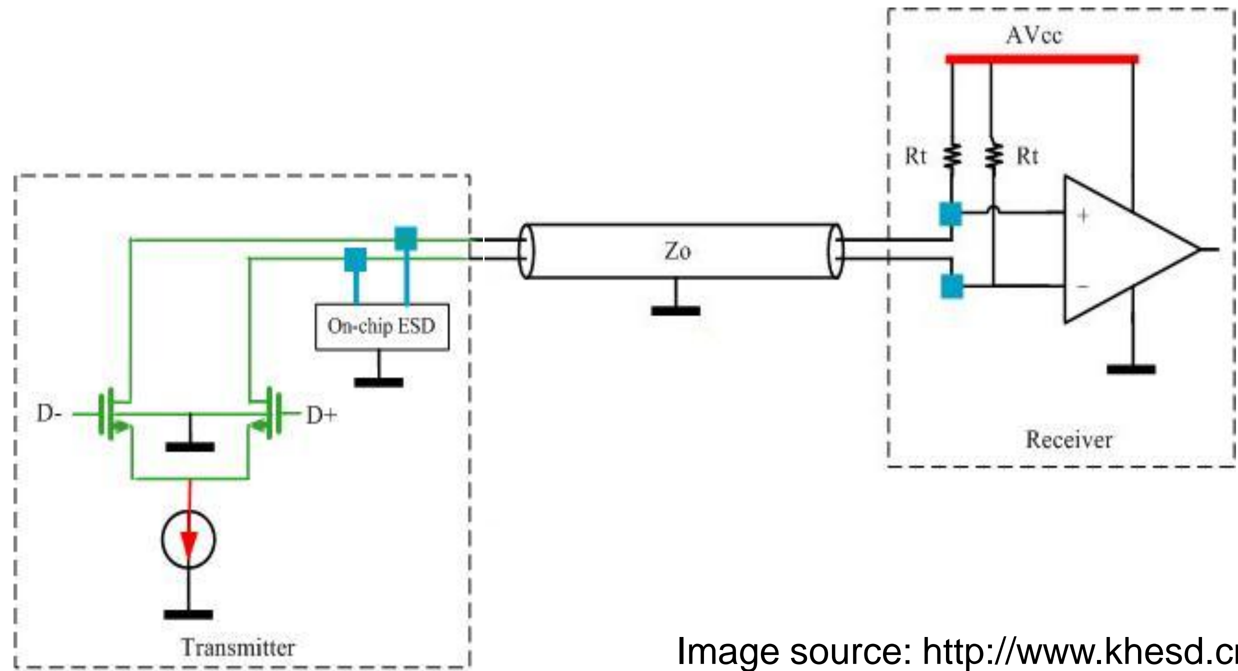


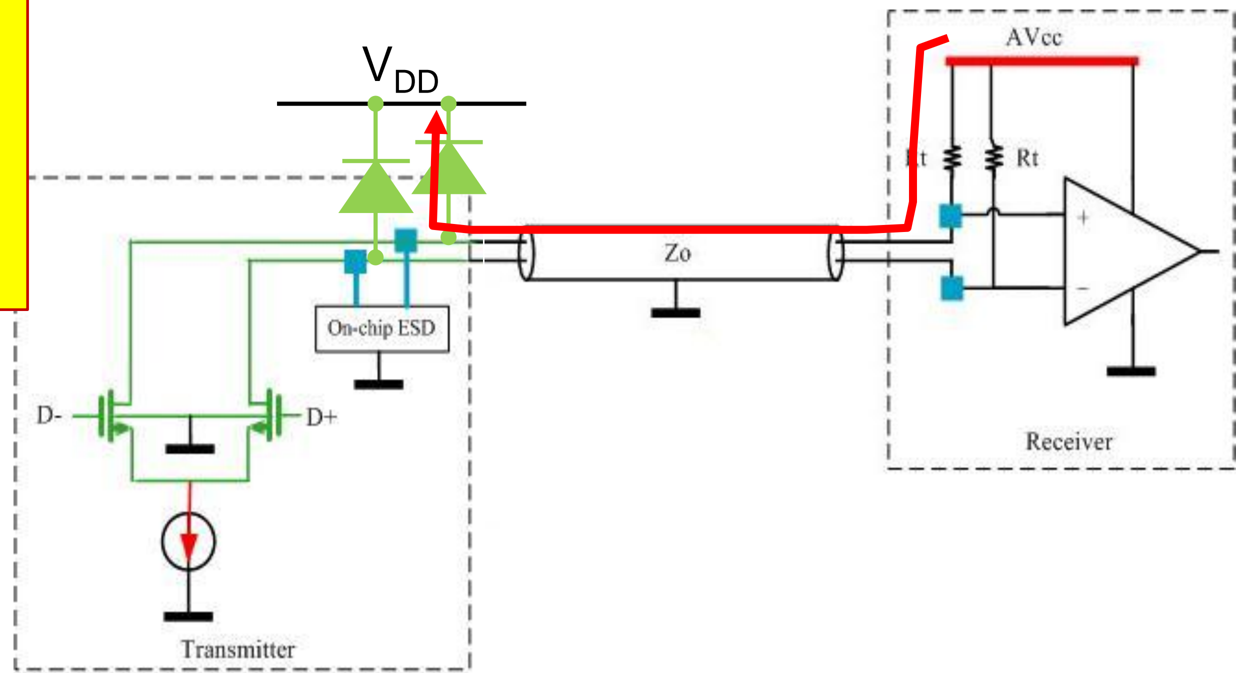
Image source: http://www.khesd.cn

Backdrive issue – unpowered sub-system

- Powered down DVD player
  - LCD TV ‘powers’ DVD player
    - Pull-up in Rx cells
    - Diode up in transmiter

Powered down ICs

Another ESD protection concept required



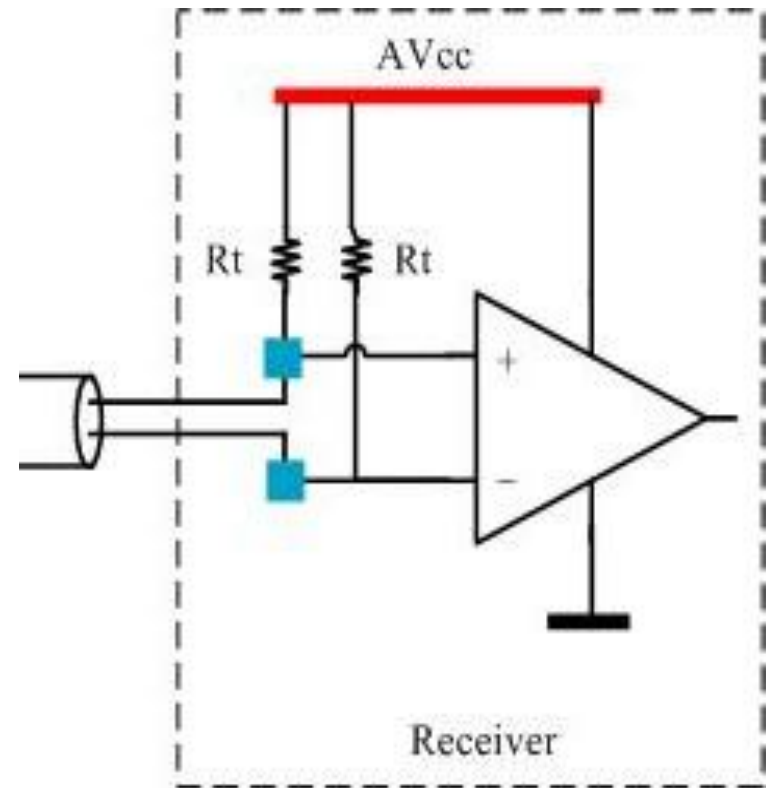
SOFICS Solutions For ICs

High speed differential communication

- HDMI TMDS interface – receiver
  - Pull-up resistance on-chip

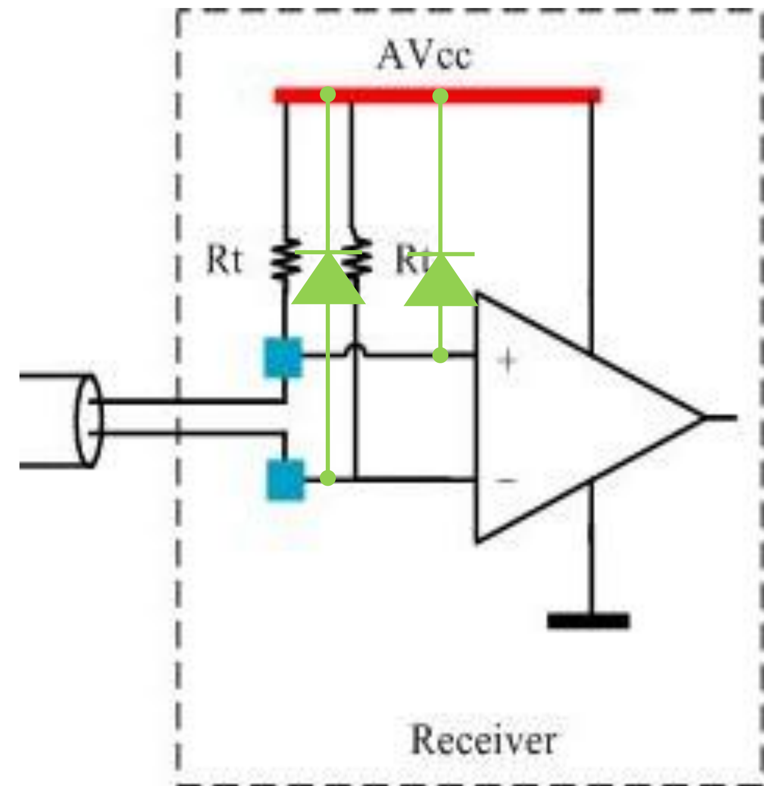
- Previous issues not relevant
  - Voltage difference: both IC at 3.3V
  - Shared bus: no problem
  - Both sides remain powered

  - Diode up still a problem?



Differential communication – diode up issue

- Diode capacitance changes Rt
  - Influences Rt value
  - Dependent on frequency, voltage
- Couples AVcc noise on pins
  - Power Supply Rejection Ratio
  - Common Mode Rejection Ratio
    - Voltage drop over both diodes not the same – capacitance differs



Diode capacitance

Another ESD protection concept required

Ref: http://www.khesd.cn

Consumer electronics – hot plug / hot swap

- Past (before 1990):
  - Shut down entire system to alter the configuration

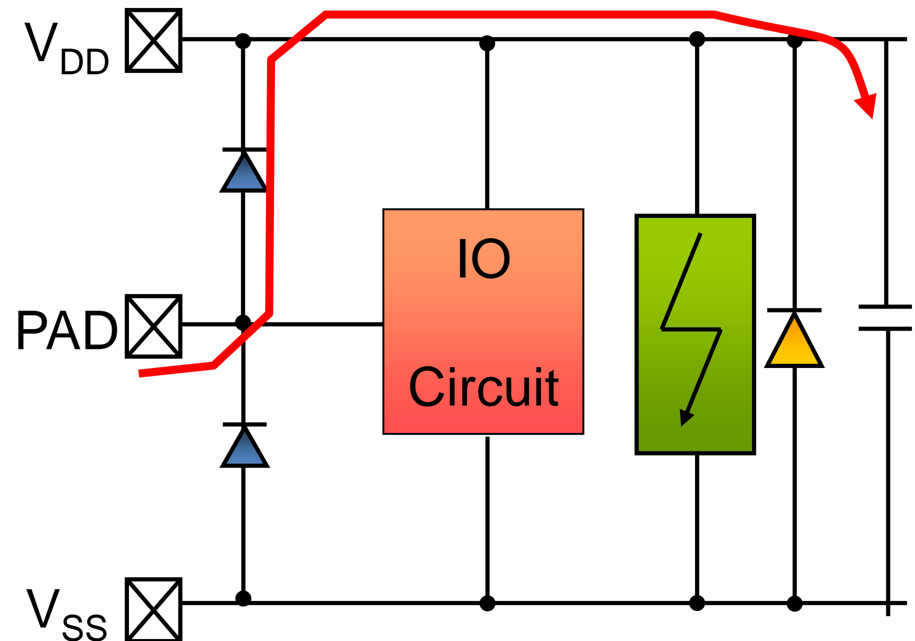
- Now: Hot plug / hot swap
  - Hot plug: expanding the system
  - Hot swap: replacing system component
  - No interruption of the system tolerated (no reboot, no restart)
  - Examples
    - USB interfaces: USB memory, USB devices
    - Raid disk driver with redundancy
    - Multimedia connections
    - Ethernet connections
    - ...

Hot swap / hot plug – diode up issue

- Hot plug: Unpowered device is connected to powered system
  - IO pins
    - Low capacitance
    - Fast charging, following IO voltage of powered systems
  - Power supply
    - Large capacitance
    - Charges more slowly

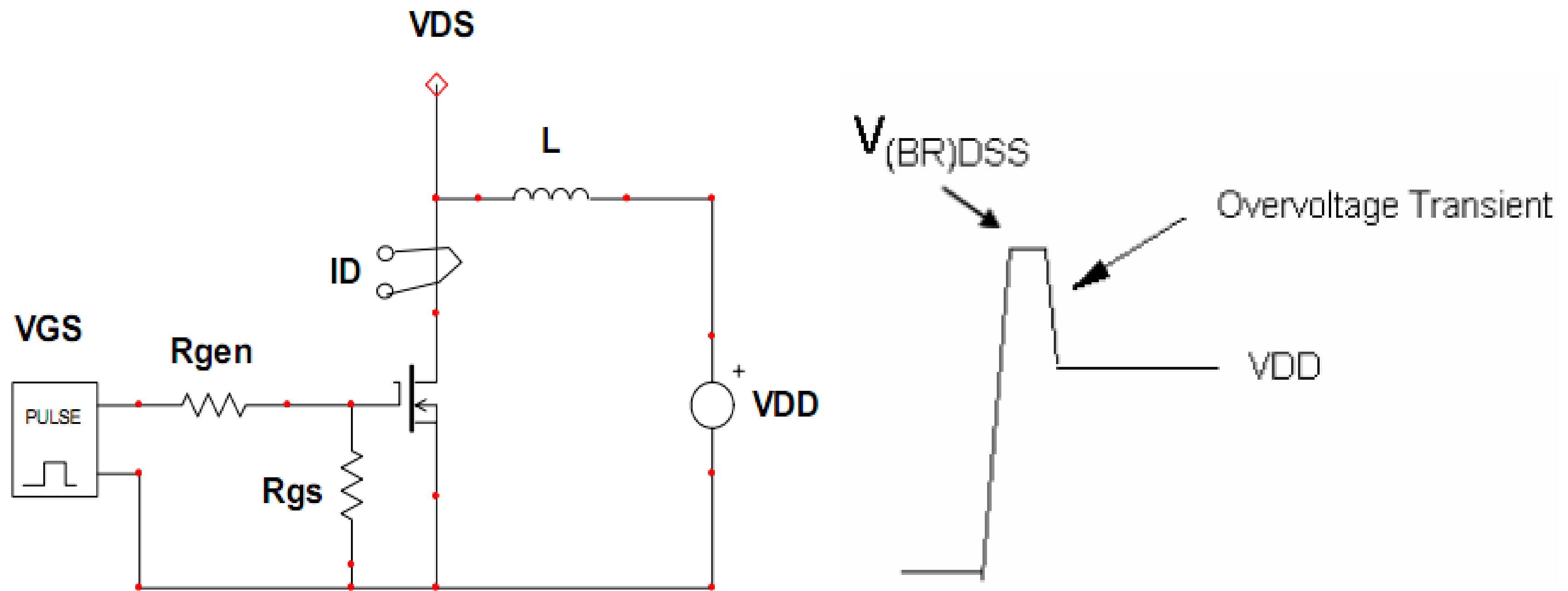
Hot plug

Another ESD protection concept required



Driving inductive loads

- Unclamped inductive switching
  - Voltage overshoot on drain-source
  - 'Diode up' not always tolerated



Ref: http://www.greatwallsemi.com/AppNotes/UIS.pdf

Electrical overstress

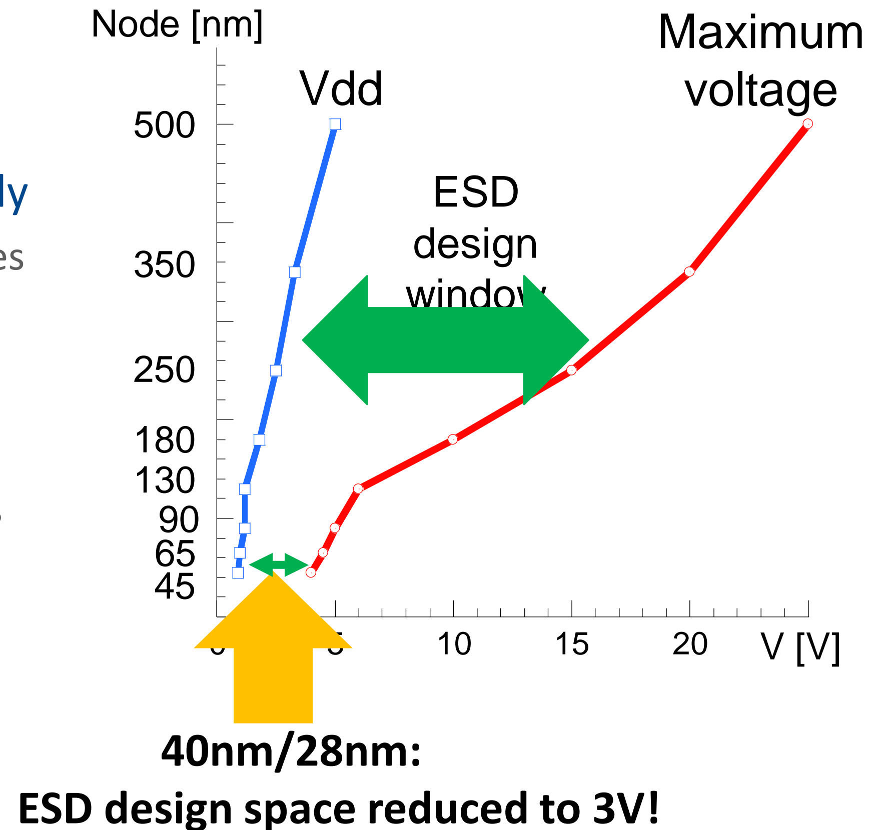
- Electrical overstress requirements
  - Example: USB 5V withstand test
    - 5V applied on D+/D- pins (3.3V interface)
    - 24hour test
    - No degradation allowed
    - Simulates damaged cable
      - 5V supply line inside USB cable shorted with high speed lines
  - Issue with ‘diode up’
    - Safest to handle the EOS stress inside the IO
    - Do not couple EOS voltage into supply line

EOS stress, inductive overvoltage

Another ESD protection concept required

Narrow design windows in advanced CMOS

- Decreasing solution space
  - Normal operation (VDD)
    - Slight decrease
  - Maximum voltage decreases rapidly
    - Transient breakdown of gate oxides
    - Burn-out of output drivers
    - Core failure voltage
  - Difference = ESD design window
    - Rapid reduction of design margins



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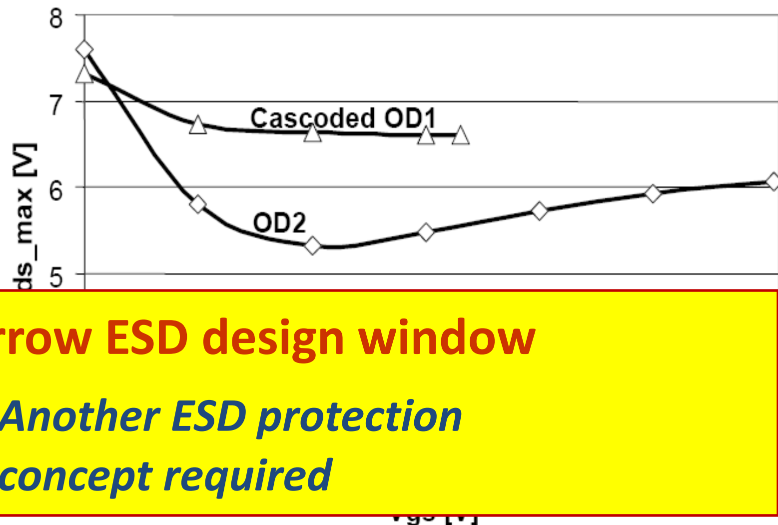
Narrow design windows in advanced CMOS

- Freescale (2006) 65nm (1.8nm / 5nm) [1.2V / 2.5V]
  - Dual diode based ESD protection with state-of-the-art rail clamp
  - GOX1: Vmax_output = 3.3V Vmax_input = 5V
  - GOX3: Vmax_output = 5.3V Vmax_input = 10V
  - Quote: "…, it is difficult to size the ESD devices to protect a single OD1 NMOSFET output buffer to 3.3V,…"



Narrow ESD design window

Another ESD protection concept required

Figure 4. V_{ds_max} data as a function of V_{gs} for the OD1 (18Å/1.2V) and OD2 (50Å/2.5V) NMOSFETs.

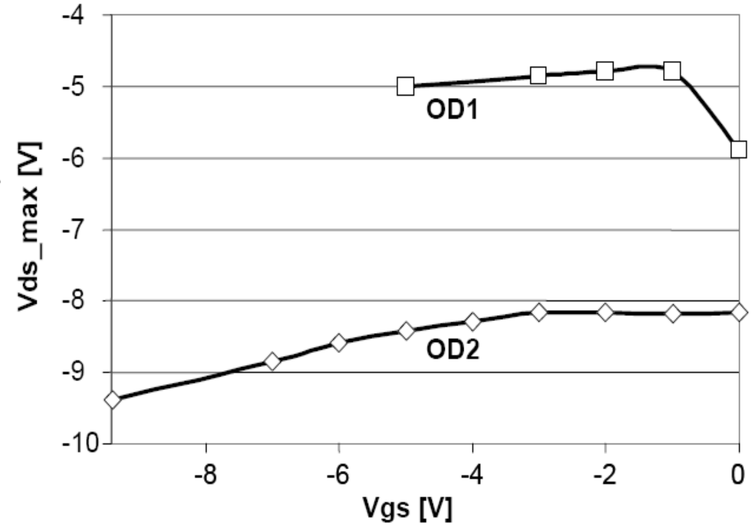


Figure 5. V_{ds_max} data as a function of V_{gs} for the OD1 (18Å/1.2V) and OD2 (50Å/2.5V) PMOSFETs.

Summary: problems caused by ‘diode up’

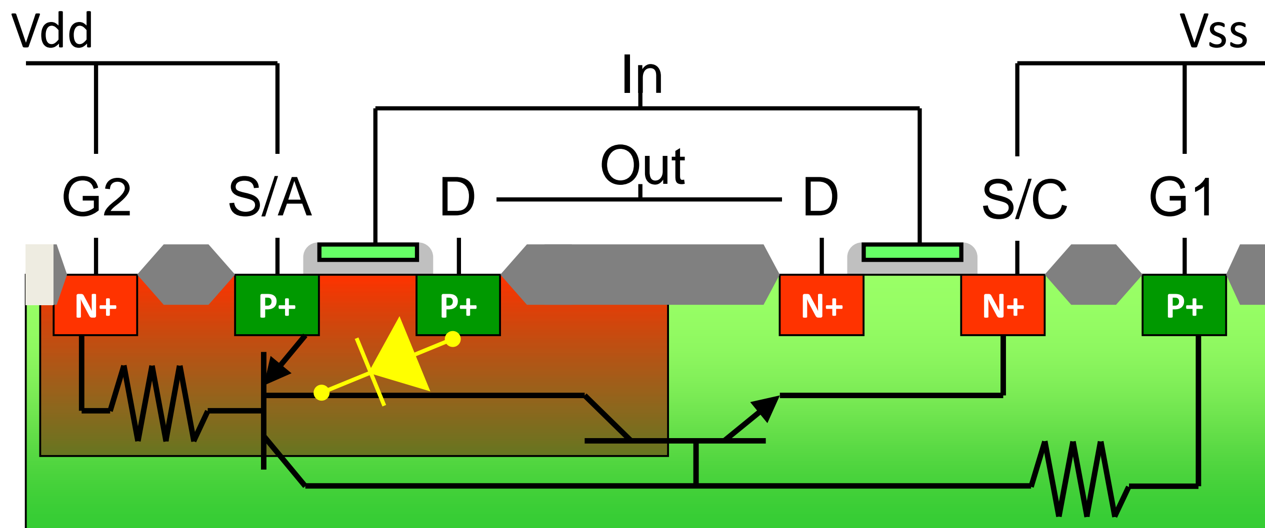
- Unwanted current flow to VDD
  - Difference in voltage level between ICs
  - Shared communication line
  - Power down of one system
  - Inductive loads
  - Electrical overstress
  - Hot swap/plug
- Unwanted diode capacitance to VDD
  - CMRR, PSRR
- Unwanted diode voltage drop
  - Thin oxide transistors in advanced CMOS

Definitions

- Open drain
  - Inverter build by on-chip MOS, off-chip pull-up resistance
  - Used in many communication shemes
- Overvoltage tolerant
  - Voltage on IO can rise above VDD level
  - ESD protection must be able to tolerate high voltage
- Failsafe
  - No interruption of shared communication line during power down of one sub-system
- Hot plug
  - Expanding the system without interruption (no reboot, no restart)
- Hot swap
  - Replacing system component without interruption (no reboot, no restart)

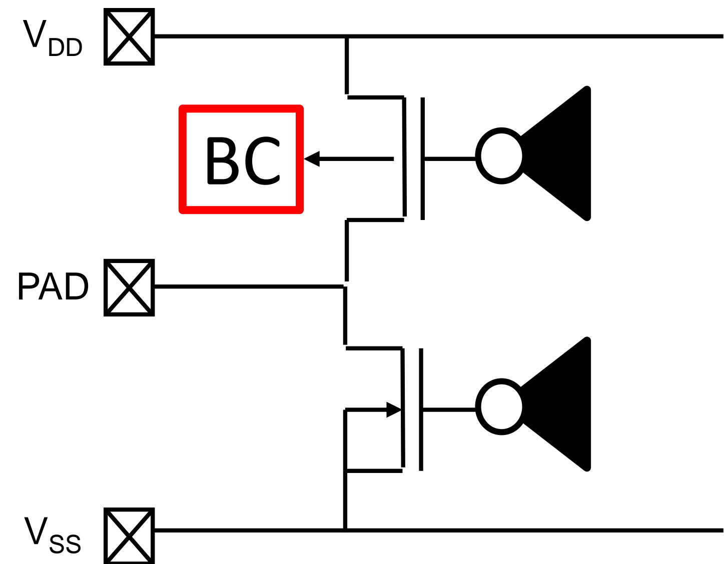
Parasitic diode up inside PMOS driver

- PMOS driver between IO-pad and VDD
  - Drain - Nwell diode
  - Diode current path must be disconnected too!



Overvoltage tolerant CMOS inverter

- Overvoltage tolerant CMOS inverter
  - Remove 'diode up'
  - Block P+/Nwell diode in PMOS
    - Nwell bias circuit (BC)
    - Several concepts patented by different companies
  - Separate gate bias pre-driver circuits
    - Shut down both NMOS and PMOS at the same time



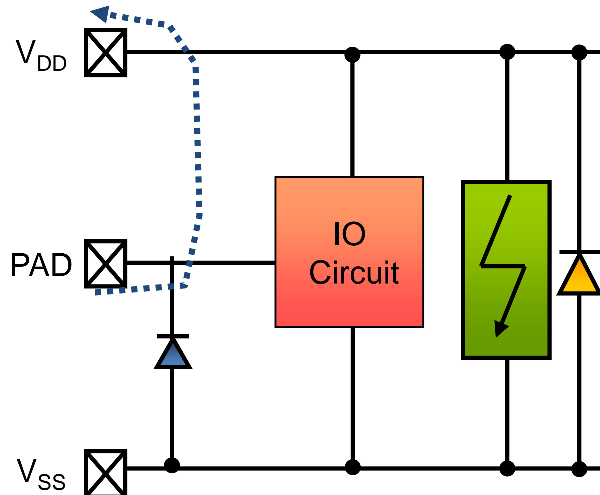
Outline of the presentation

- Introduction
- Diode up problems
- Solution concepts
  - Series diode string
  - Clamp to V_{DD}
  - Another V_{DD} reference
  - ESD bus
  - Self protective drivers
  - Local clamp to V_{SS}
- Solution examples
- Conclusion

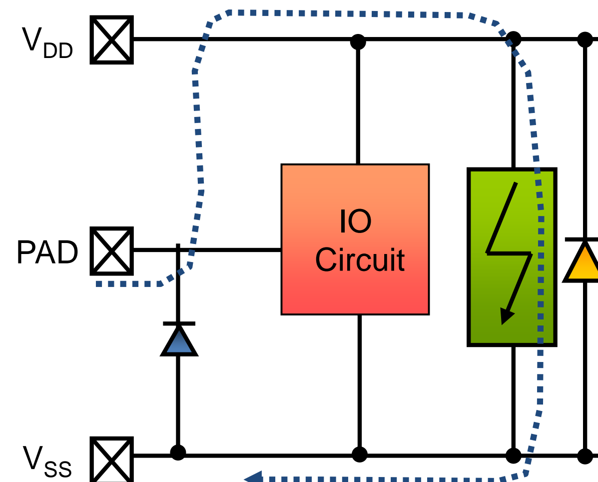
‘Diode up’ influences functional performance

- Diode up reduces IC performance
  - Action: Remove ‘diode up’
    - Stress cases PD, PS need to be covered differently

PD mode ??

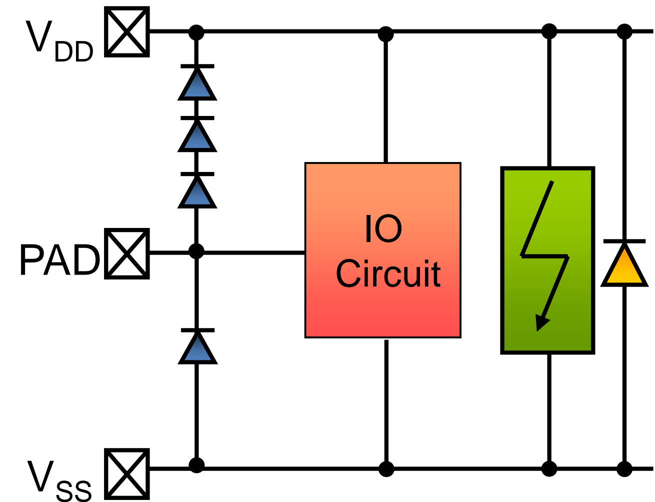


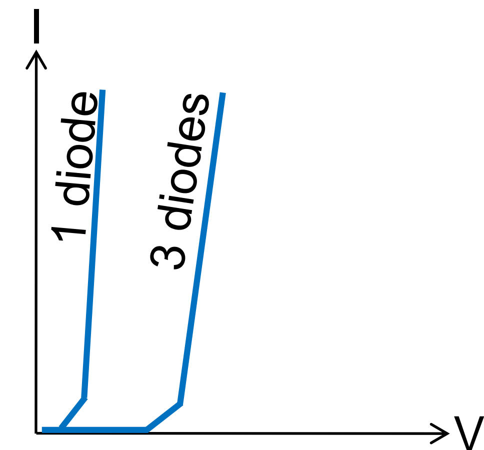
PS mode ??



Concept 1: Series connection of diodes

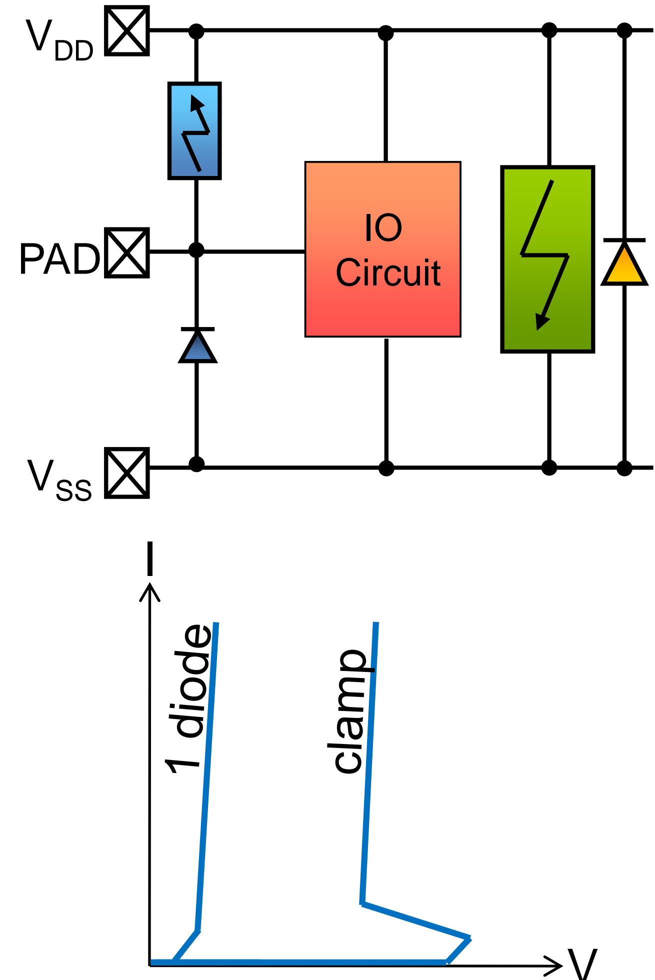
- Series connection of diodes
  - Increase the threshold for leakage from PAD to VDD
- Positive aspects
  - Simple concept
  - Small area
  - Improves capacitance
  - Low leakage
  - Tunable for specified voltage difference
- Negative aspects
  - Additional voltage drop during ESD stress
  - Not suited for sensitive IO circuits





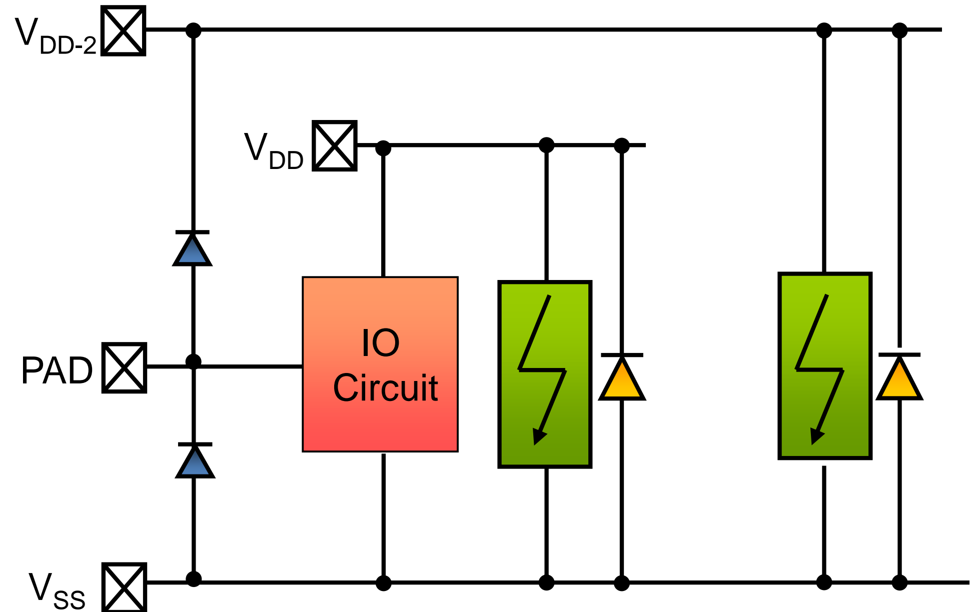
Concept 2: Clamp to V_{DD}

- Connect clamp between IO-pad and VDD
  - Increase the threshold for leakage from PAD to VDD
- Positive aspects
  - Simple concept
  - Low leakage
- Negative aspects
  - Larger area
  - Typically capacitance will increase
  - Fixed threshold – harder to change
  - Additional voltage drop during ESD stress
  - Not suited for sensitive IO circuits



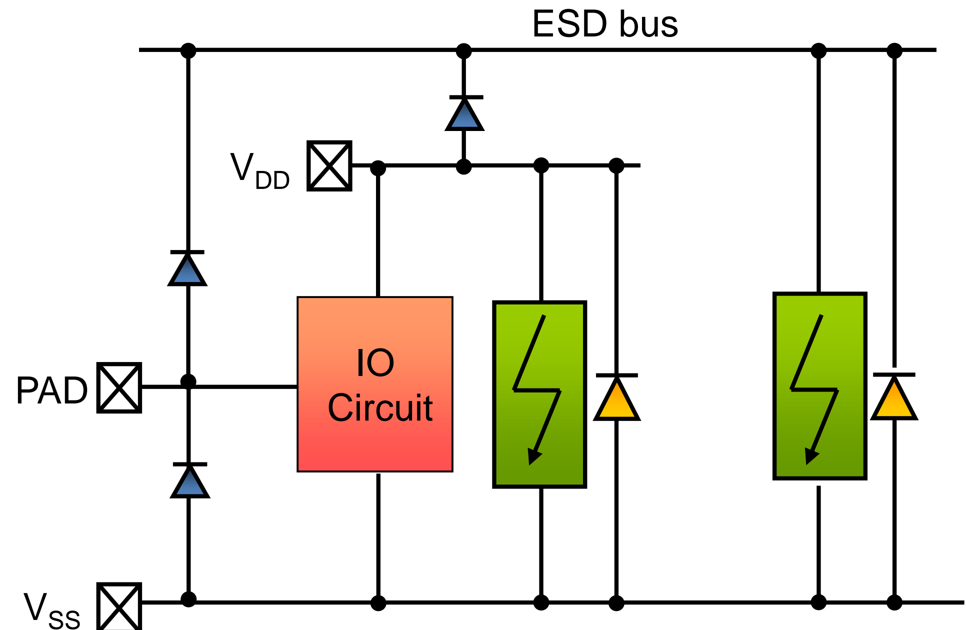
Concept 3: Separate reference

- Separate (higher) VDD
  - Another voltage reference
- Positive aspects
  - Simple concept
  - Low leakage
  - No capacitance to VDD
  - Sometimes OK for OVT
- Negative aspects
  - Many constraints for VDD-2
  - Larger area:
    - Additional bus, additional PC
  - Not suited for failsafe or hot swap
  - Sometimes not OK for OVT (PAD voltage higher than VDD-2)



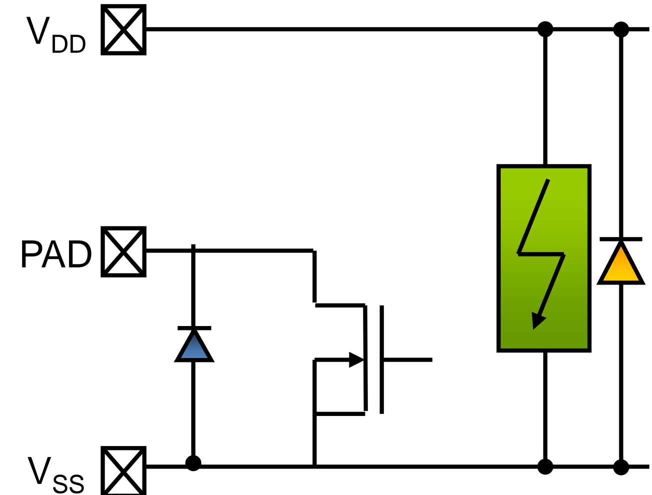
Concept 4: ESD bus

- ESD bus for VDD
  - Another voltage reference
- Positive aspects
  - Simple concept
  - Low leakage
  - No capacitance to VDD
  - OK for OVT, FS, HS
- Negative aspects
  - Larger area:
    - Additional bus, additional PC



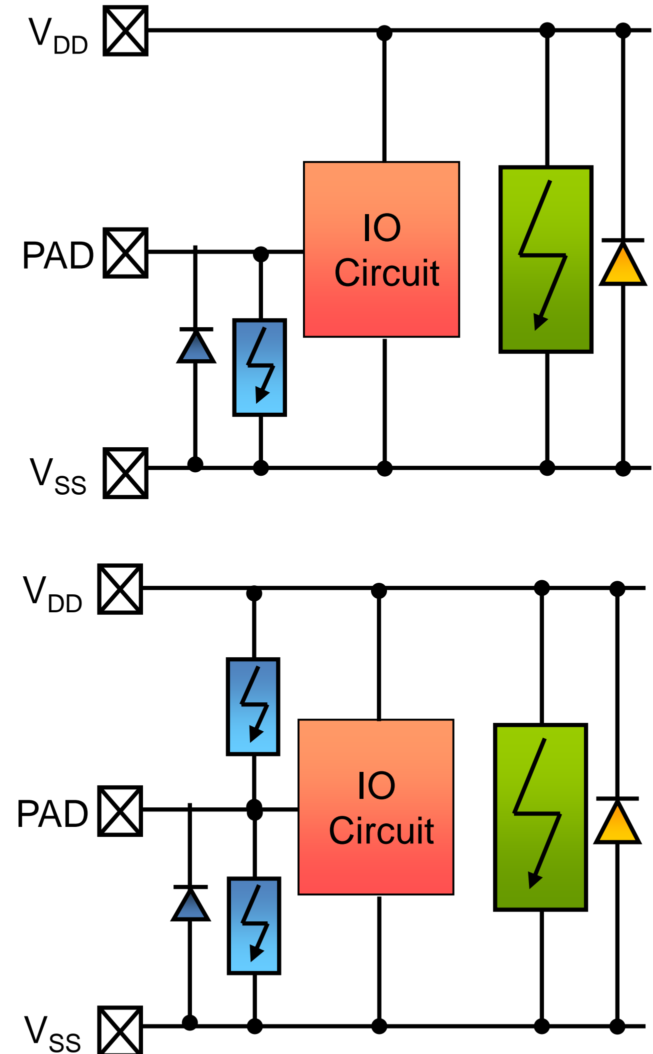
Concept 5: Selfprotective driver

- Selfprotective driver
  - Design ESD robust output driver
- Positive aspects
  - Looks like a simple concept
  - No capacitance to VDD
  - OK for OVT, FS, HS
- Negative aspects
  - Large NMOS
    - High leakage
    - Large area
  - Certainly HV MOS is typically weak during ESD stress
  - For OVT: need high voltage capable MOS



Concept 6: Local clamp protection

- Local clamp protection
  - Protect NMOS by parallel clamp device
- Positive aspects
  - Simple concept
  - Low leakage
  - No capacitance to VDD
  - OK for OVT, FS, HS
- Negative aspects
  - Medium area but many clamp concepts available



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Overview of different concepts

Concept		Overvoltage tolerant	Failsafe	Hot swap	Leakage	Capacitance to VDD	ESD Area in IO	Total ESD area
0	Dual diode	Not OK	Not OK	Not OK	Low	100%	Small	Large PC
1	Series diodes	OK	OK	OK	Low	<100%	Small	Larger PC
2	Clamp to VDD	OK	OK	OK	Low	>100%	Larger	Larger
3	VDD-2 reference	Sometimes OK	Not OK	Not OK	Low	0	Small	Larger: extra PC
4	ESD bus	OK	OK	OK	Low	0	Small	Larger: extra PC
5	Self protective	HVMOS or cascade required	OK	OK	High	0	Largest	Large
6	Local clamp	OK	OK	OK	Low	0	Medium	Small: regular PC

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Summary

- Discussed several problems with 'dual diode' ESD protection
  - Voltage level differences between ICs
  - Shared communication line
  - High speed interface
  - Hot swap
  - Backdrive protection
  - Inductive loads
  - Protection of sensitive transistors
  - ...
- Summarized solution concepts
  - Local clamp approach is most flexible – many options available

What about 'diode down'?

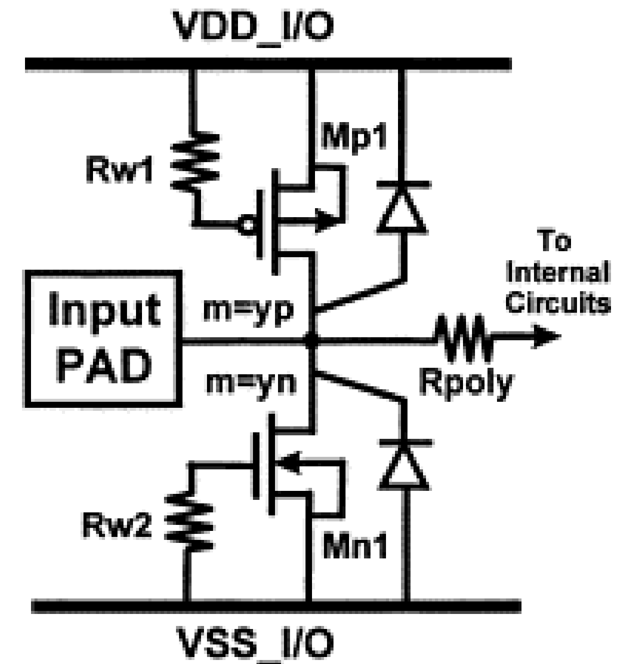
- What about 'diode down'?
  - Undervoltage tolerant interfaces
    - Automotive LIN interface needs -40V to +40V tolerance
    - Many legacy communication channels use bipolar voltage swing
    - Analog switches may need negative support too
    - RF interfaces with 'bias' voltage at 0V
  - Isolated grounds
  - Inductive loads
  - EOS stress
  - Capacitance loading
  - Narrow ESD design windows
  - ...

Outline

- Introduction
- **ESD protection for advanced CMOS**
  - Advanced CMOS nodes
  - High voltages tolerant interfaces
  - **Analog interfaces**
  - Wireless interfaces
- ESD protection in high voltage, BCD
- ESD protection in SOI technology
- Summary, conclusions

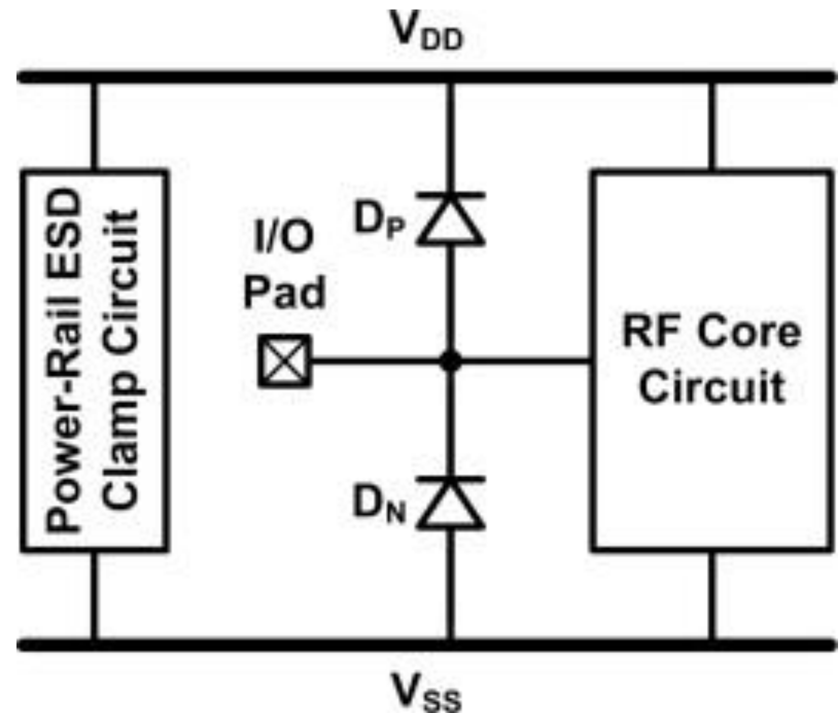
GPIO ESD concept not suitable for Analog I/O

- Typical GPIO ESD protection concept
  - ESD robust output drivers
    - Large NMOS/PMOS transistors
    - Silicide blocked drains
    - Integrated diodes
  - Poly resistance between ESD and circuit
- Issues
  - Prevent high speed circuits
  - High leakage current
  - Large silicon area
  - High parasitic capacitance



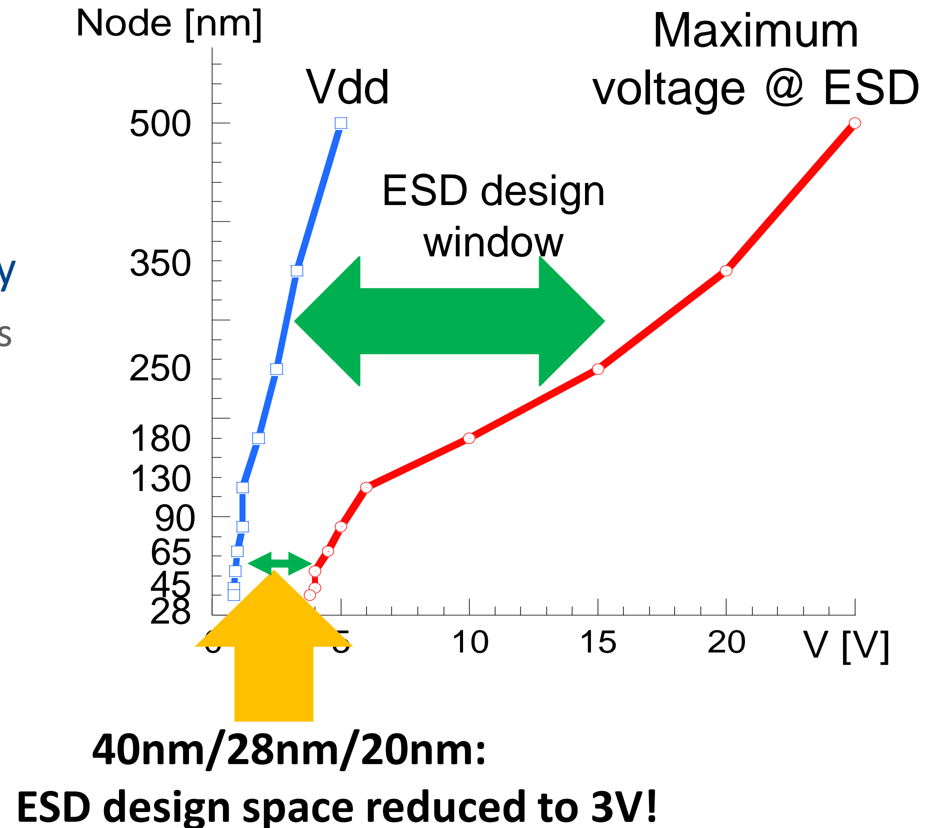
Solution: Typical Analog I/O – diode based approach

- Traditional Analog I/O
  - Simple concept
    - Diode from Vss to Pad
    - Diode from Pad to Vdd
  - Needs efficient power clamp
  - Good characteristics
    - Low leakage
    - Low parasitic capacitance
    - Small area
  - **BUT: room for improvement**
    - Lowest capacitance???
    - Overvoltage tolerant???
    - Protection of sensitive nodes???



Problem 1: Protection of sensitive nodes

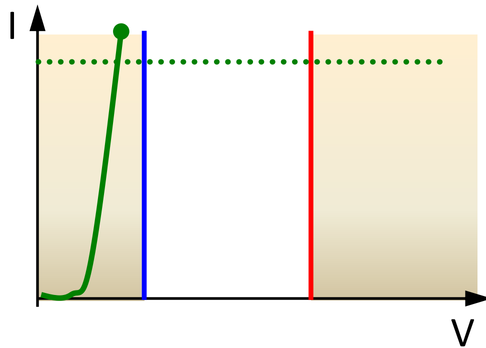
- Decreasing solution space
  - Normal operation (VDD)
    - Slight decrease
  - Maximum voltage decreases rapidly
    - Transient breakdown of gate oxides
    - Burn-out of output drivers
    - Core failure voltage
  - Difference = ESD design window
    - Rapid reduction of design margins



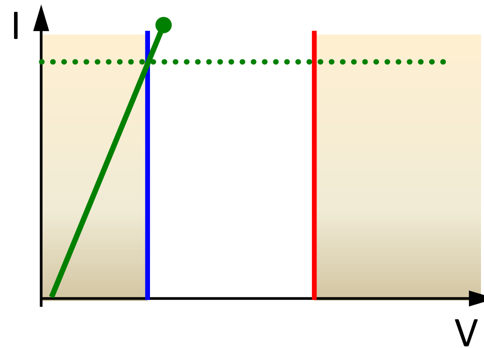
40nm/28nm/20nm:
ESD design space reduced to 3V!

‘Dual diode’ protection difficult in advanced CMOS

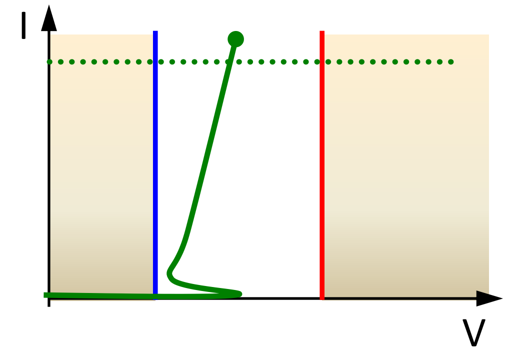
Diode

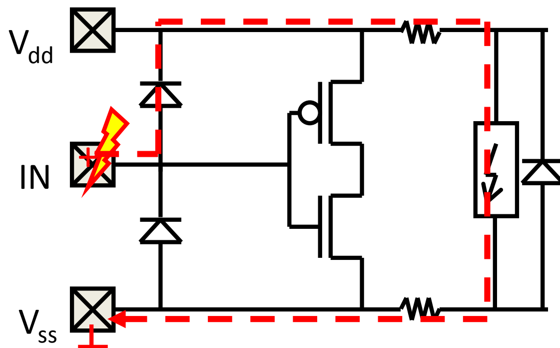


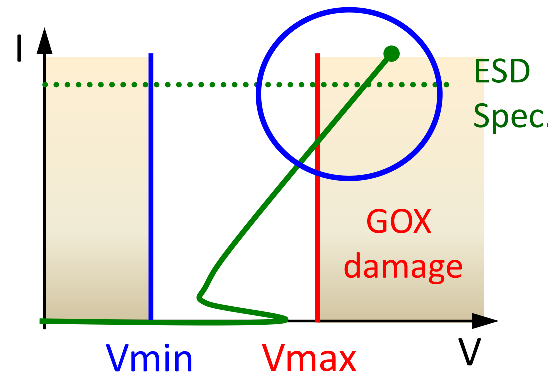
Resistance of Vdd, Vss bus line



Power Clamp





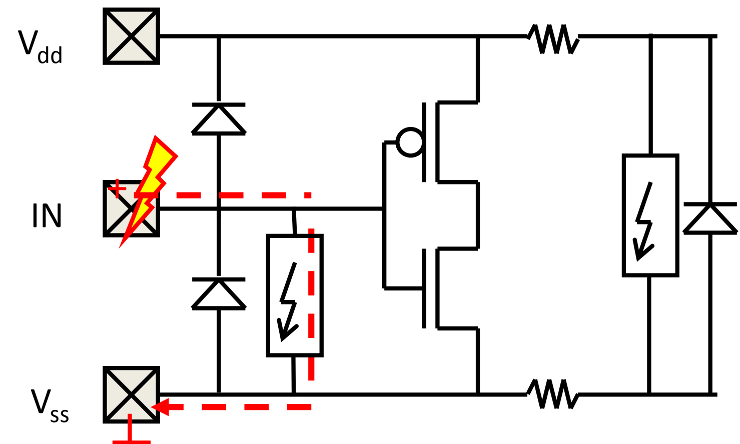


Robustness: OK

Effectiveness: NOT OK

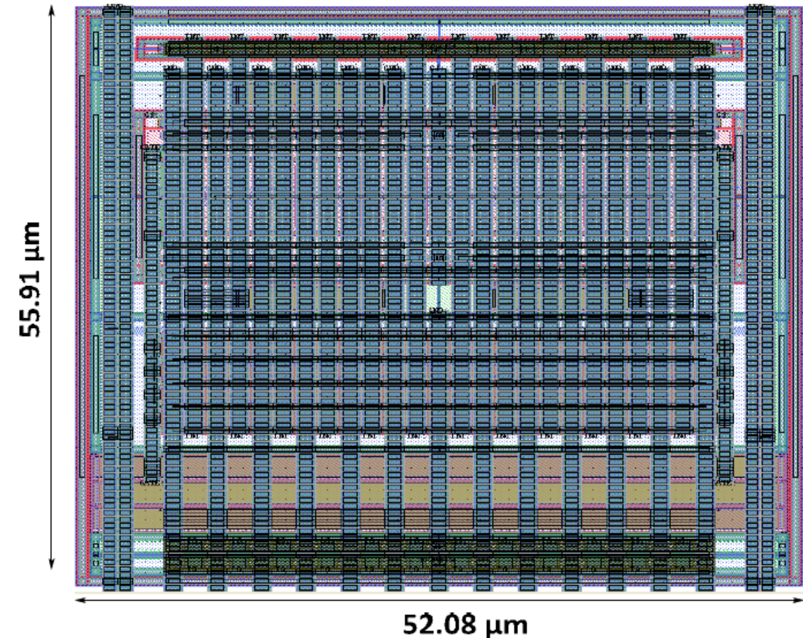
Solution: Local I/O clamp reduces total voltage drop

- Local I/O clamp
  - Strongly reduce voltage drop during ESD
  - Many different device options
  - Place power clamp in the I/O !?
- Concerns?
  - Leakage current at I/O?
  - Parasitic capacitance at I/O?
  - Silicon footprint?
  - Latch-up immunity?



Example: Local I/O clamp protects RF-IO, TSMC 90nm

- ESD protection for LNA IO
  - ESD: >2kV HBM
  - Latch-up immune
  - Low capacitive: <100fF
  - Low leakage: <0.1nA
  - Small area: <3000um^2
  - CUP: ESD under bond pad



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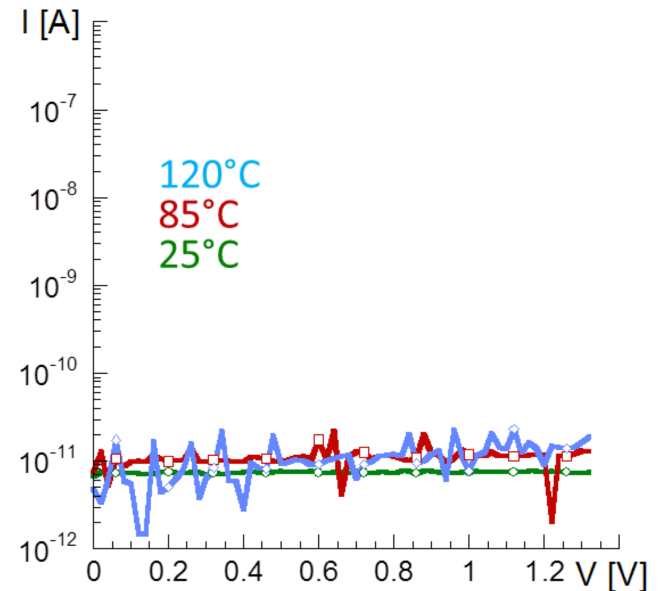
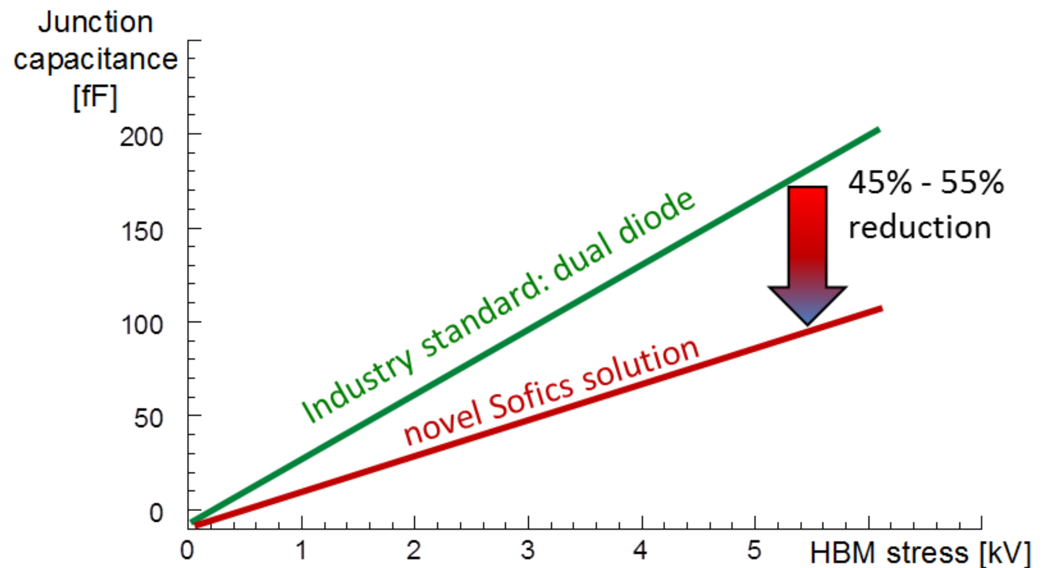
Examples: protecting low leakage analog interfaces

- Reduce ESD related leakage with proprietary ESD IP
  - Example: 1.2V TSMC 40nm
    - ESD protection for RF LNA circuit
    - Leakage ~20pA at 1.2V at high temperature
  - Example: 5V TSMC 180nm
    - ESD protection for overvoltage tolerant IO
    - Leakage ~10nA at 5V at high temperature
  - Example: 65nm ESD cells
    - All kinds of voltage domains
    - All kinds of interface types
    - Leakage ~20nA at high temperature



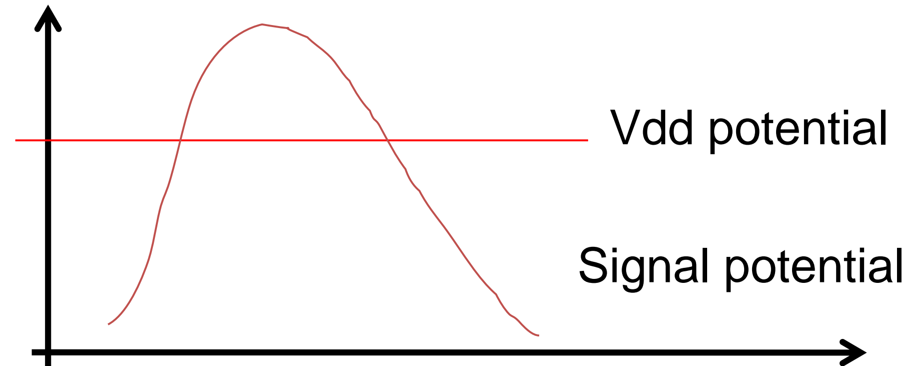
Example: I/O ESD with low parasitic capacitance

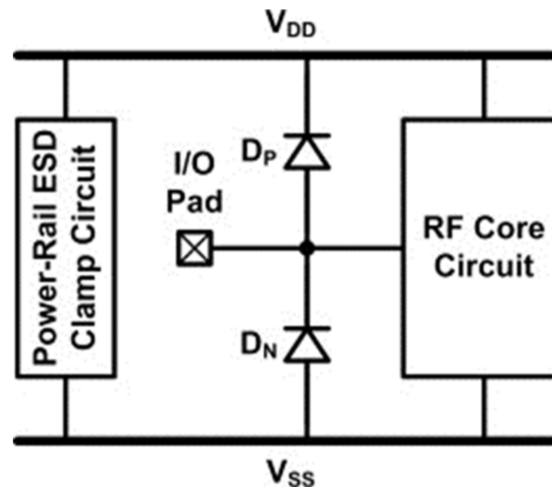
- Innovation: Local ESD with ultra low parasitic capacitance
  - Parasitic capacitance
  - Silicon proven
    - 65nm: - 45%
    - 28nm: - 55%
  - Reduce cap for same ESD
  - Increase ESD for same cap



Another issue with diodes: Signal voltage limitation

- Problems introduced by diode from Pad to Vdd
  - Voltage level differences between ICs
  - Shared communication line
  - High speed interface
  - Hot swap
  - Back drive protection
  - Inductive loads
  - …

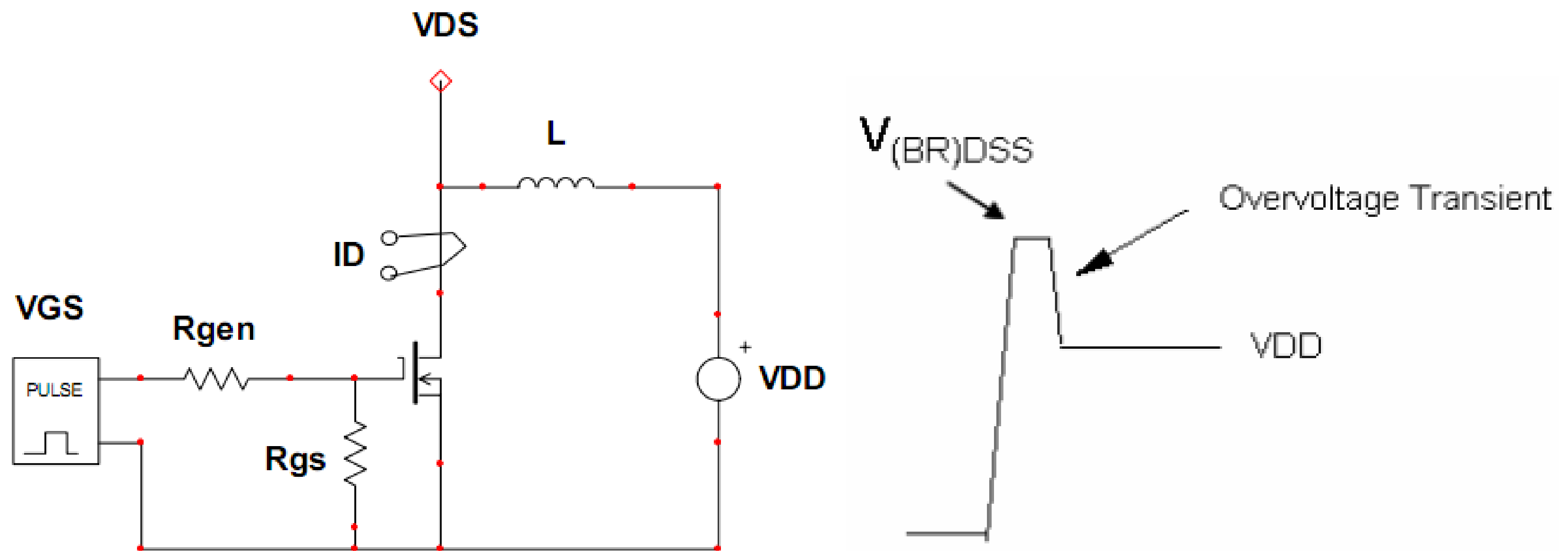




SOFICS Solutions For ICs

Inductive switching creates voltage over shoot

- Unclamped inductive switching
  - Voltage overshoot on drain-source
  - ‘Diode up’ not always tolerated



Examples: Protect high voltage capable/tolerant IOs

- Sofics proprietary clamps for high voltage / overvoltage tolerant interfaces
  - 3.3V based on 1.8V – SD/SIM card — 40nm + 28nm
  - 5V based on 3.3V – HDMI — 130nm
  - 5V tolerant IO's – TCON (LCD panel) — 180nm + 130nm
  - 5V tolerant IO's based on 3.3V – HDMI — 130nm
  - 15V flash protection — 65nm
  - 15V based on 5V – Battery charger — 0.25um
  - **NEW:** 4V, 5V, 6V and even >10V protection — 28nm

Summary: Several issues with traditional Analog I/O

- Unwanted current flow to VDD
  - Difference in voltage level between ICs
  - Shared communication line
  - Power down of one system
  - Inductive loads
  - Electrical overstress
  - Hot swap/plug
- Unwanted diode capacitance to VDD
  - CMRR, PSRR
- Unwanted diode voltage drop
  - Protect sensitive thin oxide transistors in advanced CMOS

Outline

- Introduction
- **ESD protection for advanced CMOS**
  - Advanced CMOS nodes
  - High voltages tolerant interfaces
  - Analog interfaces
  - **Wireless interfaces**
- ESD protection in high voltage, BCD
- ESD protection in SOI technology
- Summary, conclusions

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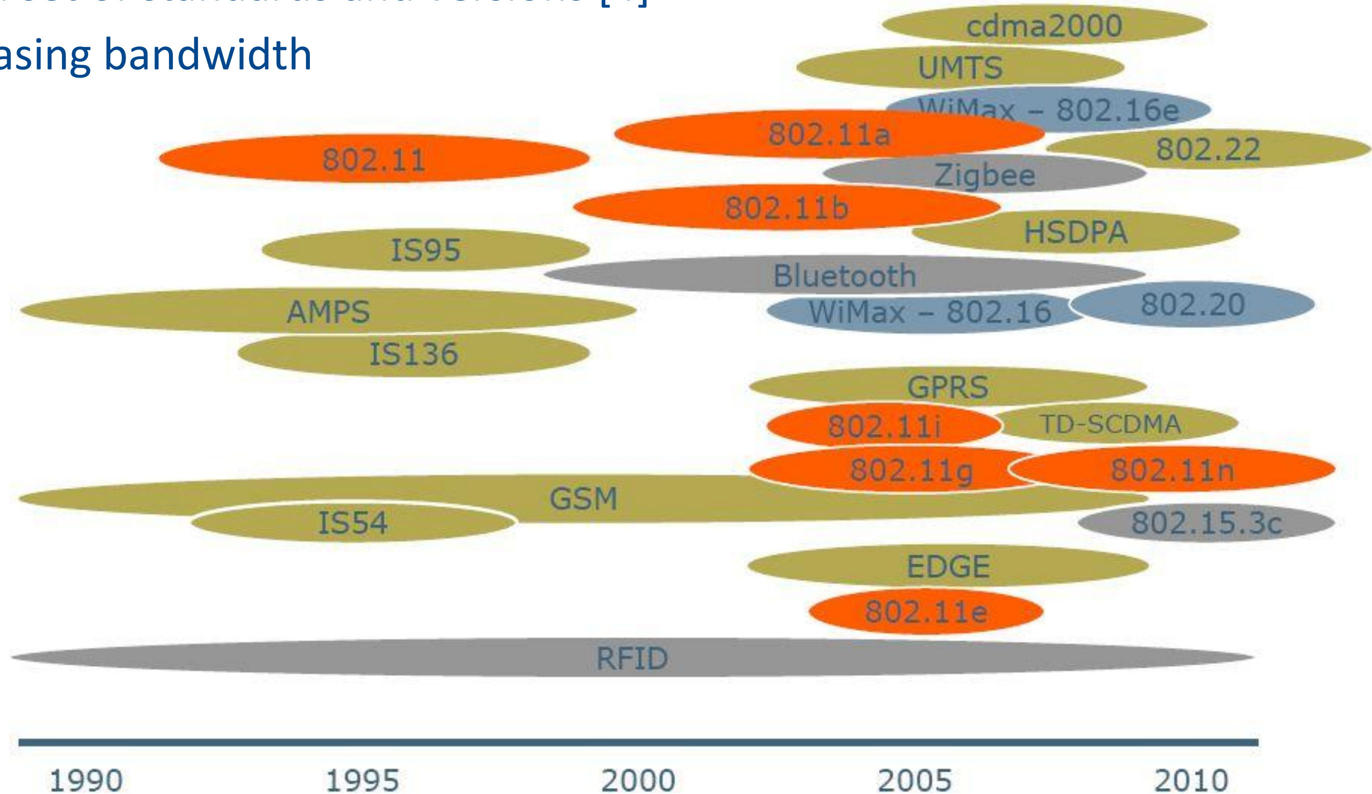
Intro: History

"I do not think that the wireless waves I have discovered will have any practical application."

– Heinrich Rudolf Hertz (1857–1894)

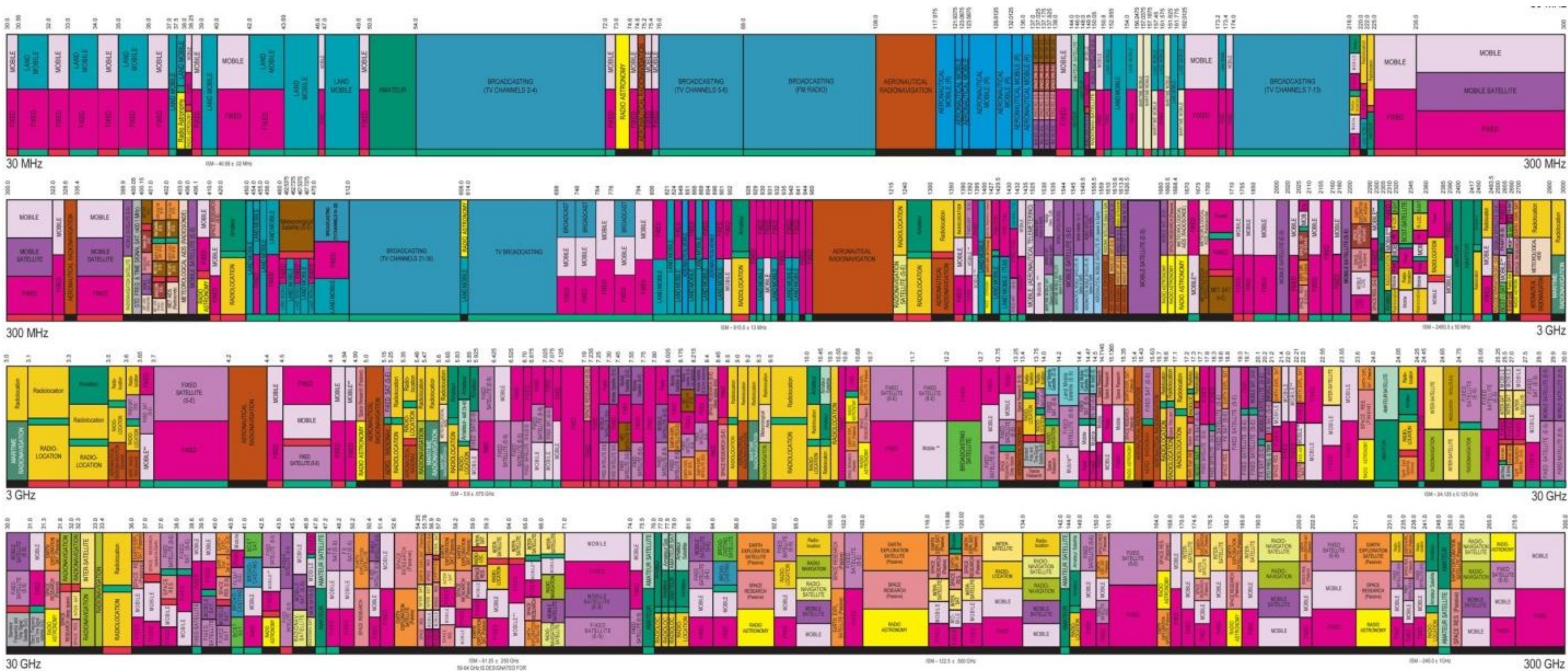
Intro: Explosive growth of wireless interfaces

- Wireless interfaces: very diverse and growing [3]
  - Broad set of standards and versions [4]
  - Increasing bandwidth



Intro: Available spectrum hard to find

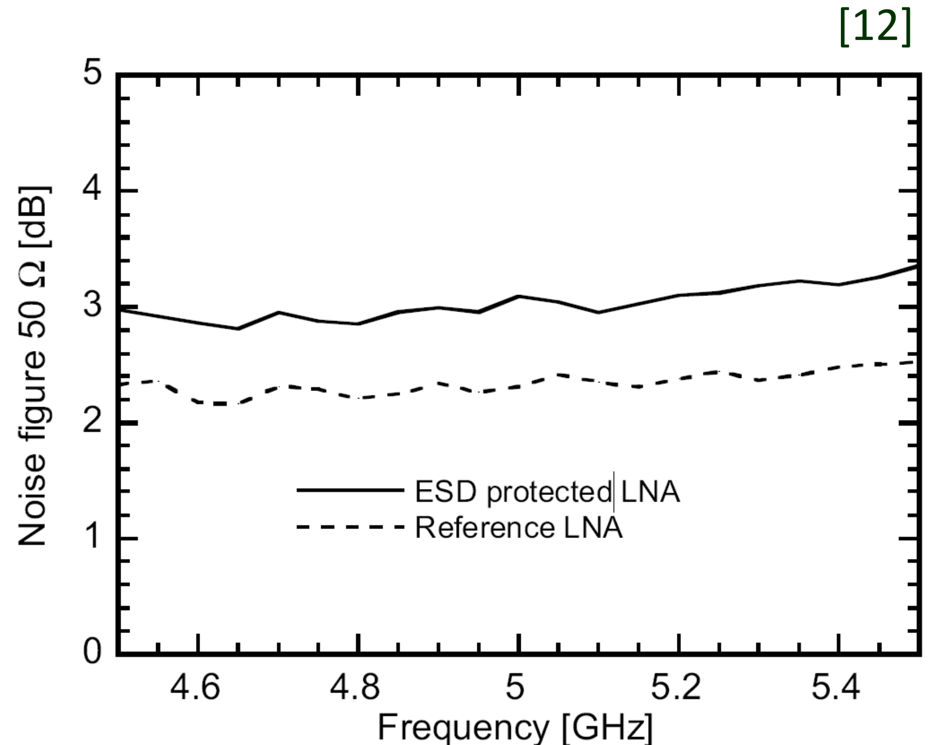
- Example: US spectrum almost completely assigned [2]
  - Many wireless protocols/versions: need generic ESD solutions



Intro: ESD protection influences RF performance

- Example: RF ESD protection
  - Lower gain (S21)
  - Higher noise figure (NF)
  - Degraded input reflection coefficient (S11)
- Unique ESD solutions required
  - Low parasitic capacitance
  - Low pad resistance
  - High Q factor
  - Low leakage

[12]

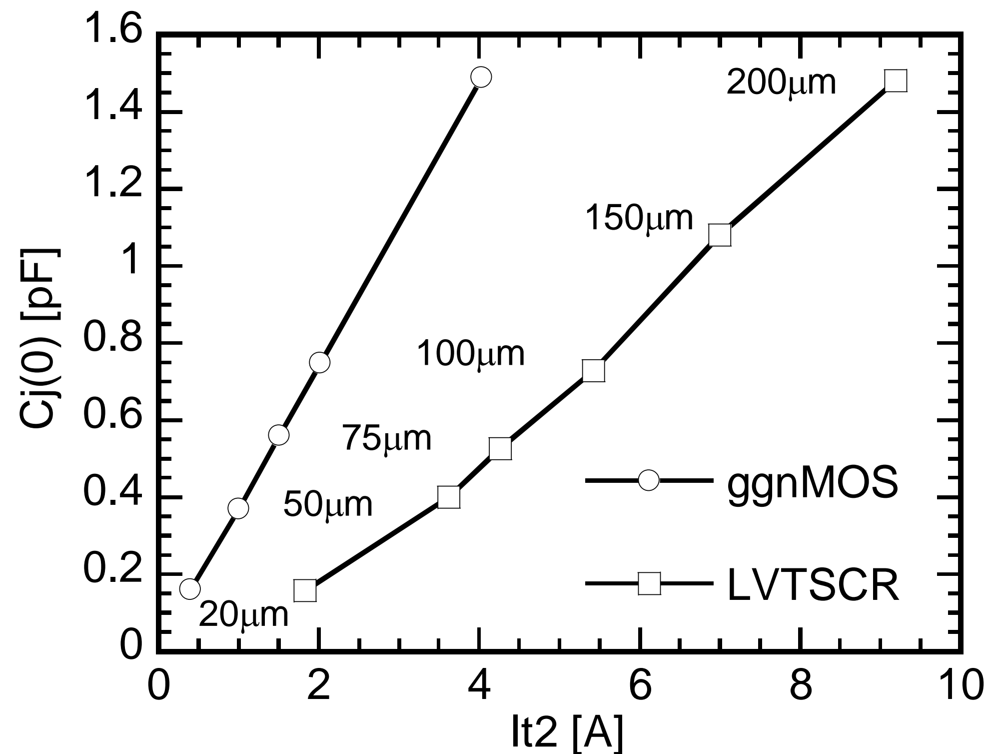


Outline

- Introduction
- **Protection approaches**
  - **Plug-n-play**
  - **LC cancellation**
  - **ESD-RF Co-design**
- 90nm product
- 40nm product
- Conclusion

Approach 1: Plug-n-play

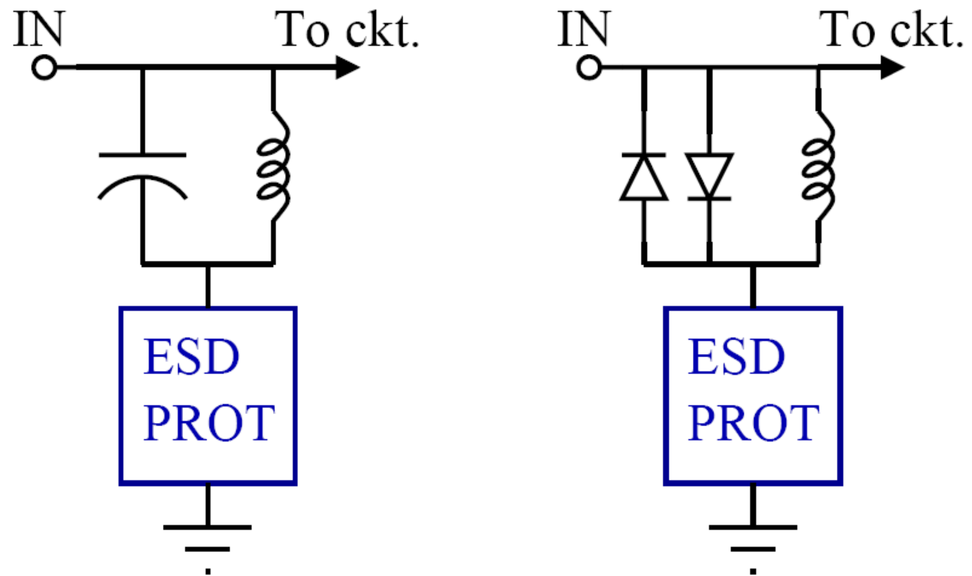
- Minimize parasitic capacitance of ESD devices
  - Parasitic capacitance chosen not to degrade RF performance
  - Most used approach:
    - dual diode and efficient power clamp
  - Alternative:
    - Local protection clamps
    - Select optimal protection device [15-21]



Approach 2: LC cancellation

- ESD protection using filters and cancellation
  - LC resonator isolates the ESD protection device from the RF input
  - Resonator is tuned to the operation frequency of the RF circuit
  - Does not require high-Q ESD protection device

- References [10, 13, 22]



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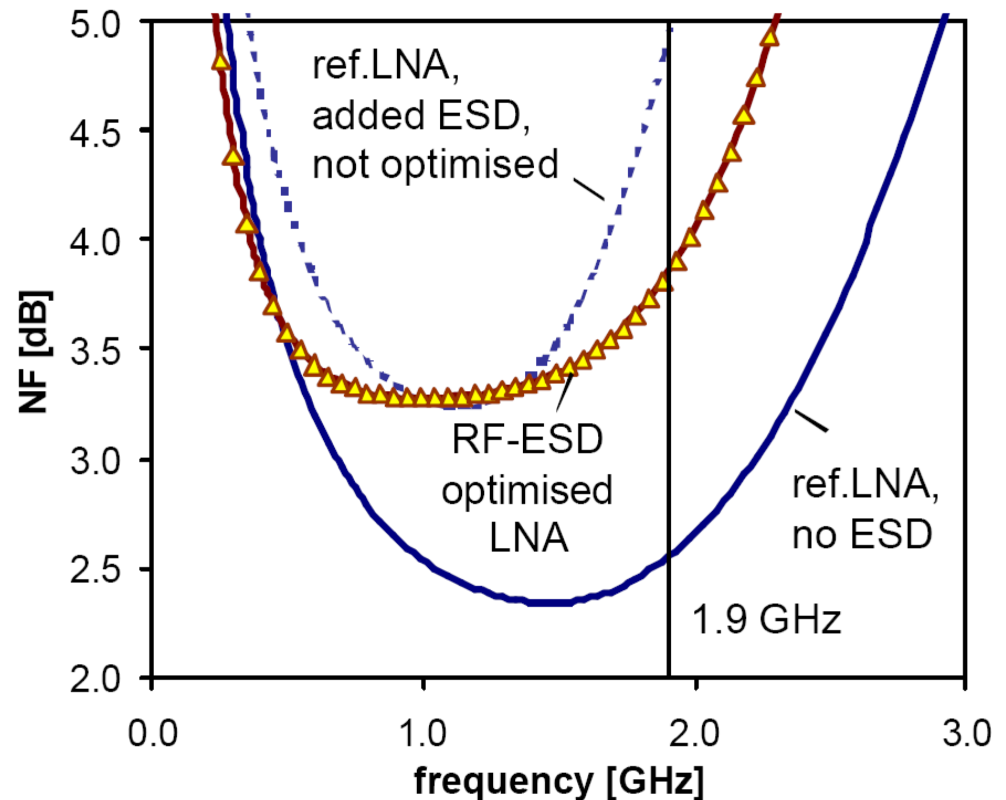
Approach 3: ESD – RF co-design

- Full (or partial) circuit ESD co-design
  - ESD protection is integrated in RF design
  - More designer freedom
  - Designer has to know both RF and ESD!

- References [23, 24]



SOFICS Solutions For ICs

Plug-n-play approach selected in this work

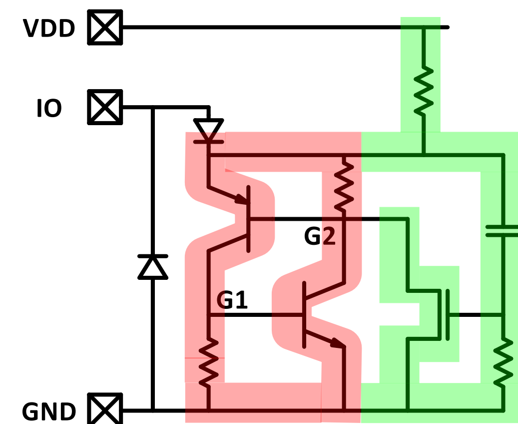
- Researchers claim "low-cap. plug-n-play" is limited to 5GHz
  - References: 10, 13, 22-24
- This presentation contradicts these claims
  - Plug-n-play approach proven for 8.5GHz in TSMC 90nm
  - Solutions measured up to 20GHz in TSMC 40nm LP
  - Solutions:
    - Proprietary silicon controlled rectifier clamps
    - Low capacitive loading
    - Low leakage – High Q
    - No pad resistance

Outline

- Introduction
- Protection approaches
- **90nm product**
  - **Application**
  - **Protection concept**
  - **Results**
- 40nm product
- Conclusion

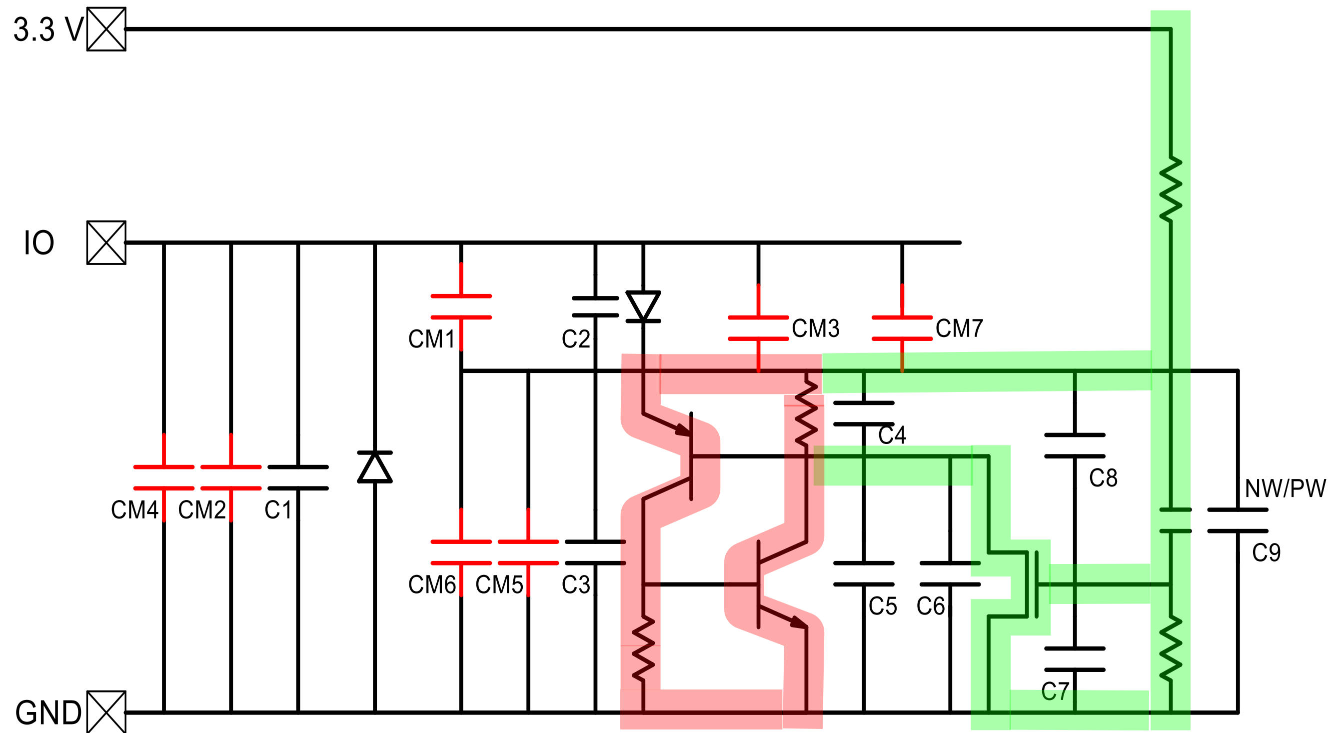
90nm product: 8.5 GHz LNA

- Application: RF - tagging
  - 8.5GHz wireless interface
  - Location aware
  - 10 year lifetime from 1 coin battery
  - 802.15.4a standard: Alternate PHY for Zigbee devices
- Protection concept
  - Design window failure voltage: 11.4V
  - Dual diode approach not possible
    - Only narrow Vdd connection available
  - Local clamp
    - SCR triggered by dynamically biased MOS



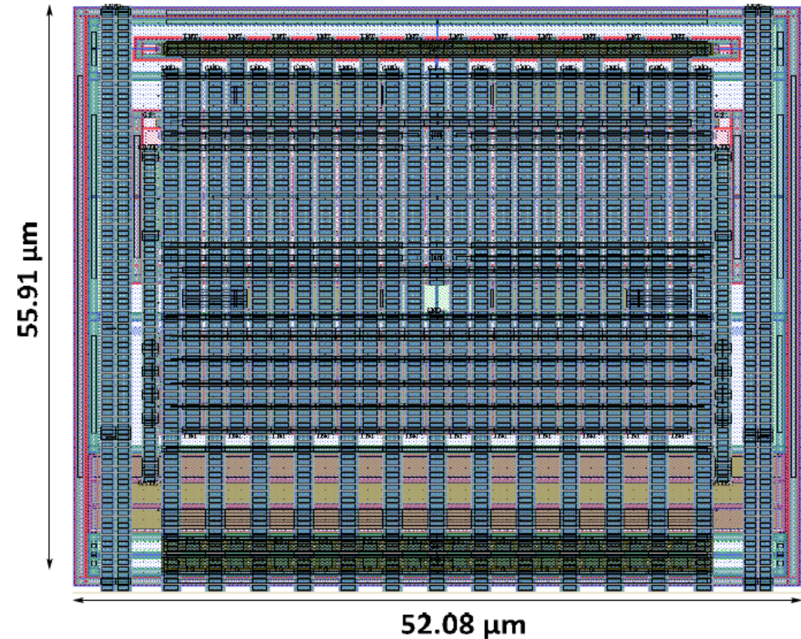
90nm product: Capacitive loading

- Parasitic capacitance: calculation based on foundry data
  - Maximum 100fF allowed



90nm product: Results

- ESD protection for LNA IO
  - ESD: >2kV HBM
  - Latch-up immune
  - Low capacitive: <100fF
  - Low leakage: <0.1nA
  - Small area: <3000um^2
  - CUP: ESD under bond pad

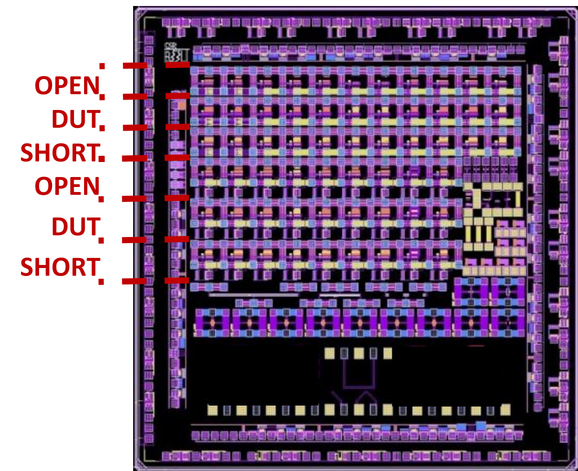


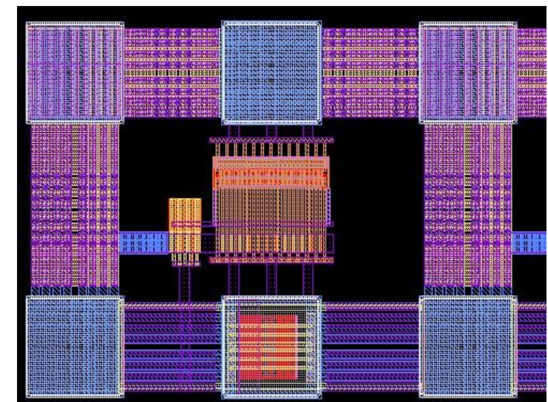
Outline

- Introduction
- Protection approaches
- 90nm product
- **40nm product**
  - **Application**
  - **Protection concepts – comparison**
  - **Solution selection**
- Conclusion

40nm product: GPS/Bluetooth application

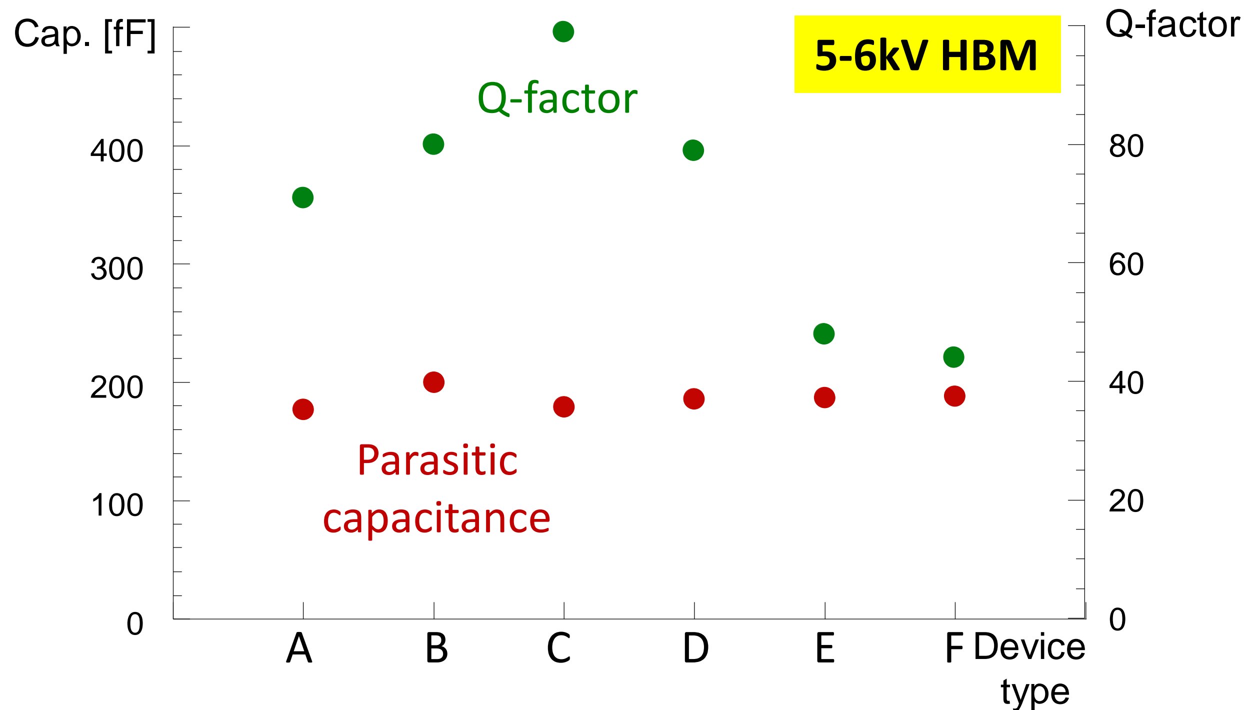
- Application in 40nm
  - Bluetooth interface
  - GPS interface
- ESD protection for LNA IO
  - Compared various ESD concepts
  - S-Parameters measured from 1 to 20GHz
- Requirements
  - Capacitance < 200fF
  - Q-factor > 40
  - 2kV HBM





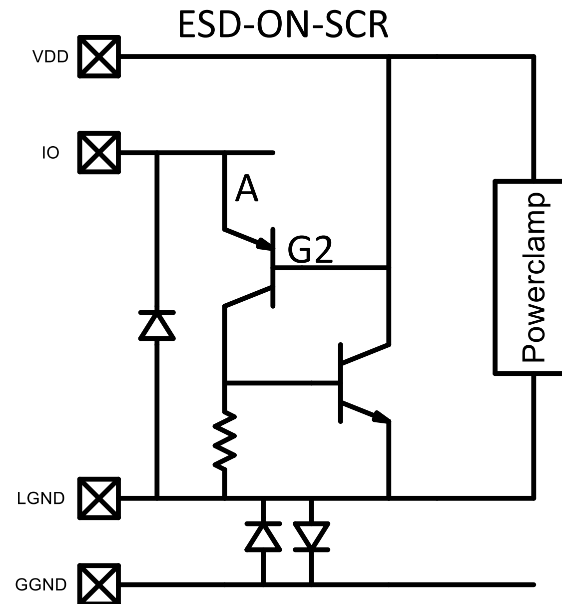
40nm product: Various protection concepts

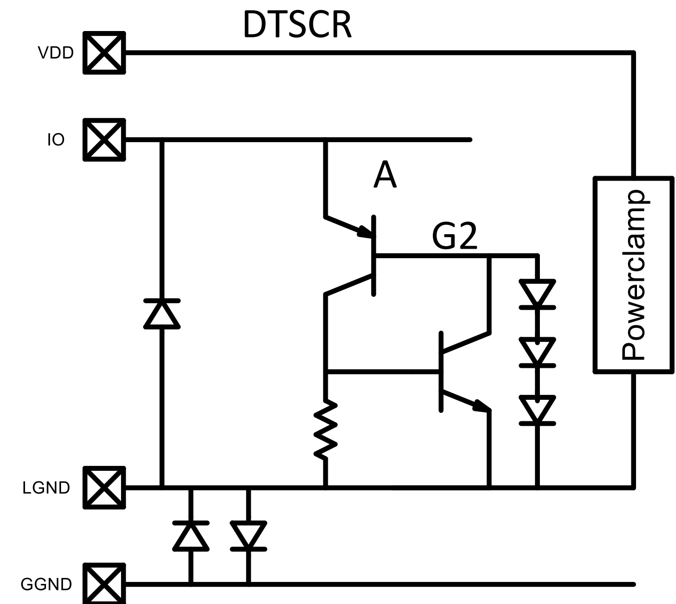
- Various ESD device types investigated for high speed RF applications
  - Low parasitic capacitance, high Q-factor, high ESD performance



40nm product: Comparison of 2 device types

- Comparison of final selected devices
  - ESD-on-SCR
  - DTSCR

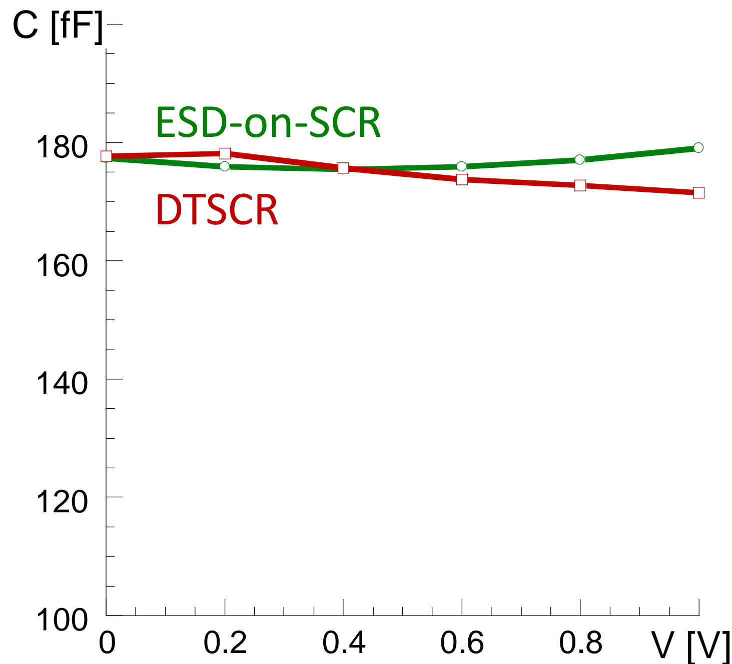


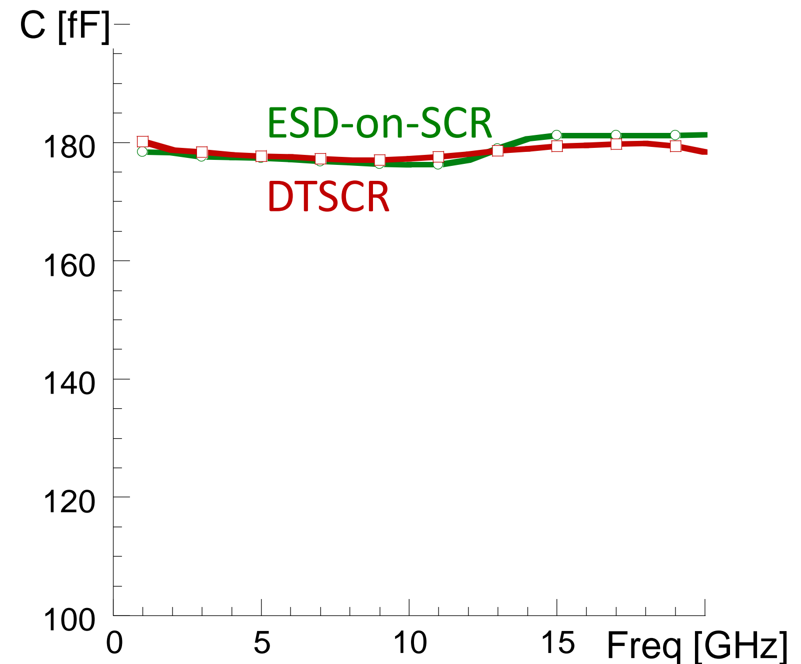


40nm product: S-parameters comparison

- Stable behavior for two finally selected protection devices

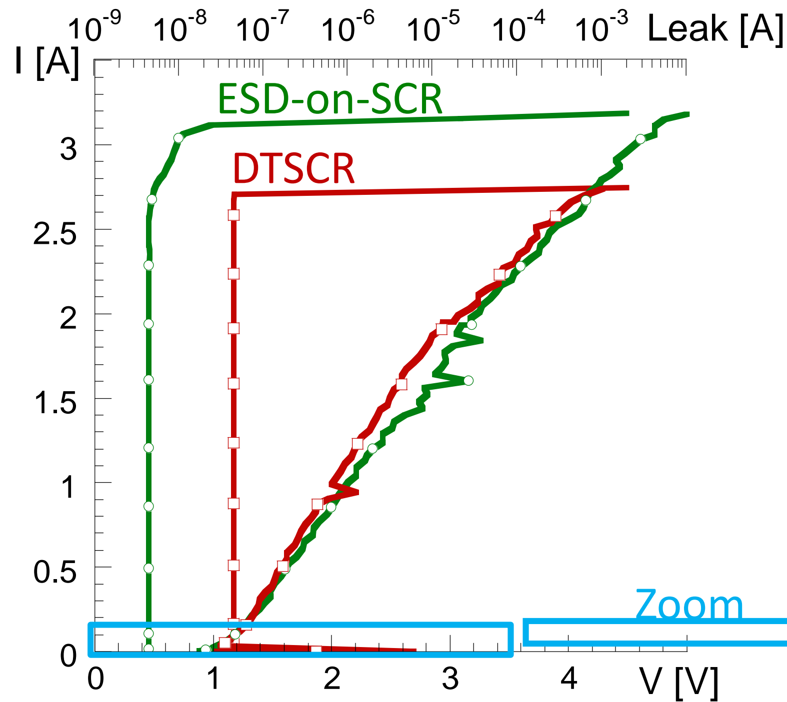
across voltage (@ 5GHz) and across frequency (@ 0V bias)

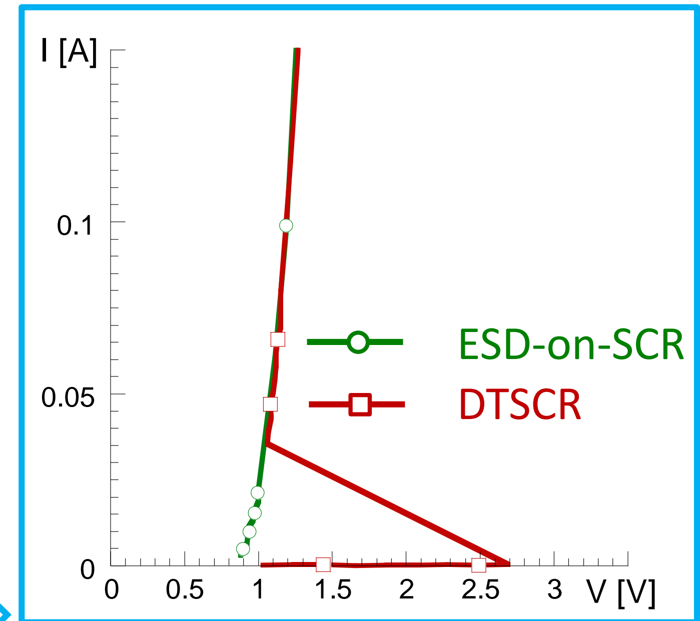




40nm product: TLP comparison

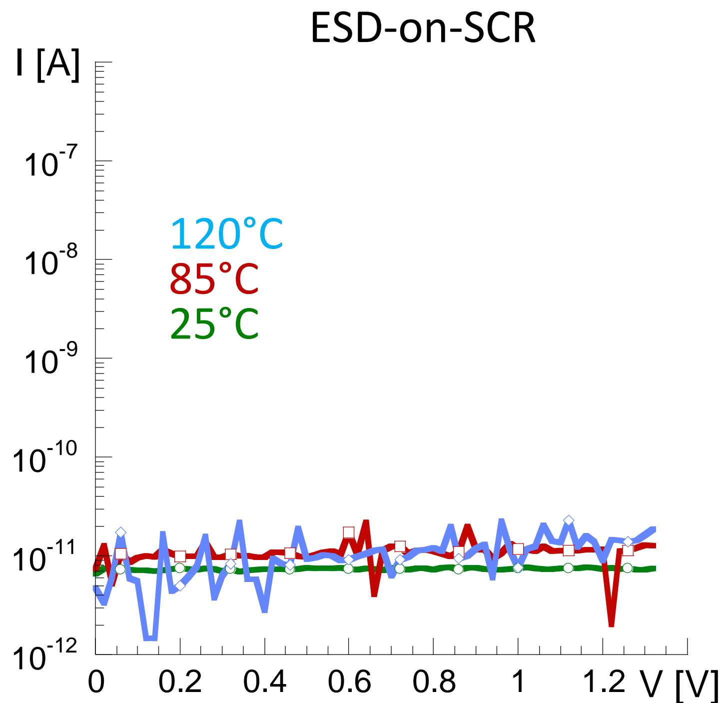
- TLP results
  - Same failure level ~2.6A
  - Lower trigger voltage for ESD-on-SCR

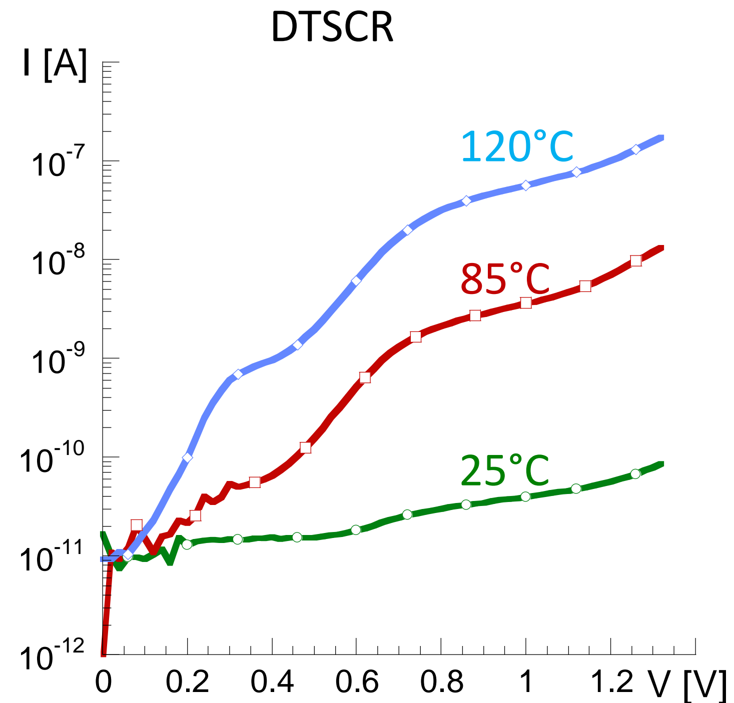




40nm product: Leakage comparison

- Leakage:
  - ESD-on-SCR has much lower leakage





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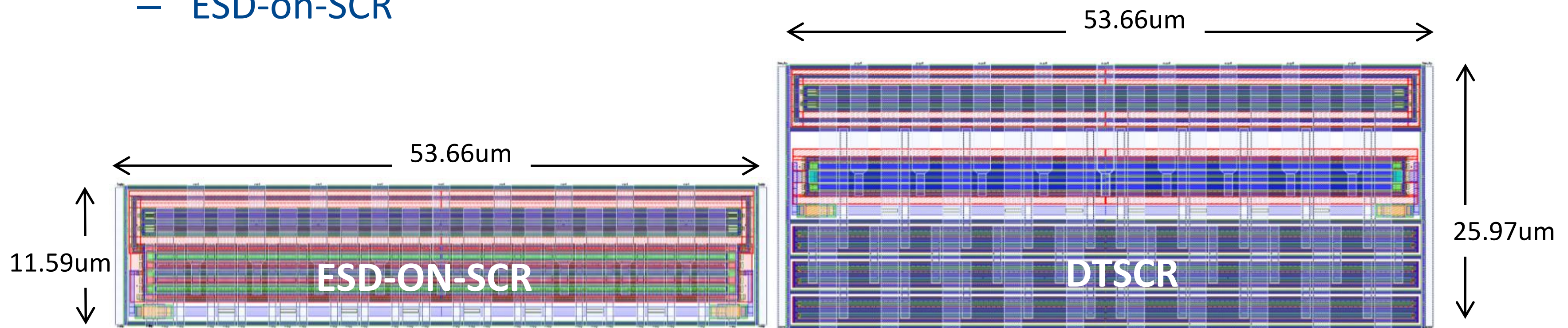
40nm product: Comparison summary

- Comparison summary
  - DTSCR
  - ESD-on-SCR

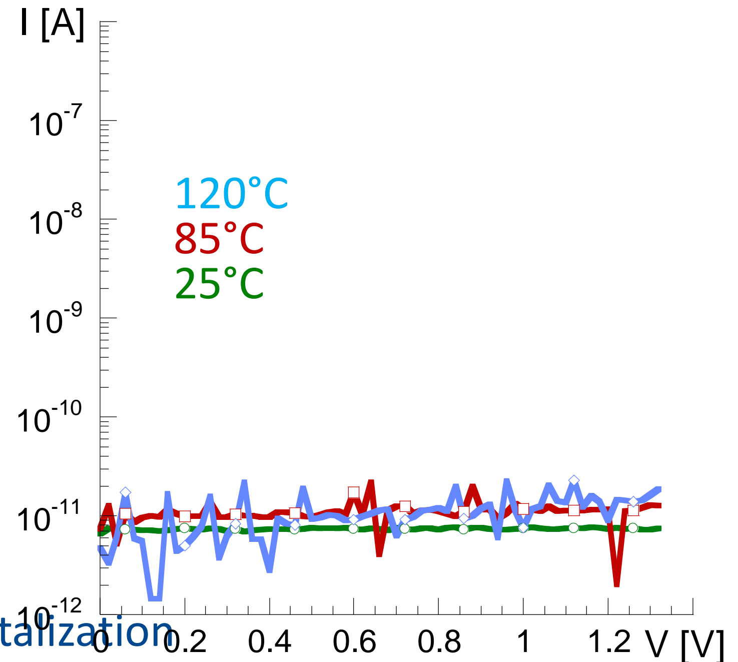


Device	Leakage @ 1.32V			Parasitic capacitance			Q-factor	Area [um²]	ESD performance		
	25°C [A]	85°C [A]	125°C [A]	Total [fF]	To VSS [fF]	To VDD [fF]			HBM [kV]	MM [V]	TLP [A]
ESD-on-SCR	7.5p	12.7p	18.5p	177	116	61	**71**	622	5.2	300	2.51
DTSCR	85.3p	13.2n	174.0n	178	170	**8**	43	1286	4.5	240	2.59

especially desirable for common mode power rejection ratio

40nm product: Selected solution: ESD-on-SCR

- ESD-on-SCR: Ideal for small signal RF LNA circuit
  - Leakage 10pA
  - Parasitic capacitance* 180fF
  - Q-factor 71
  - ESD performance 5.2kV
  - Silicon area 622um²



* S-parameter measurement including metalization

Outline

- Introduction
- Protection approaches
- 90nm product
- 40nm product
- **Conclusion**

Conclusion

- Summary
  - SCR based ESD protection for LNA's for Bluetooth, IEEE802.15.4a
  - Measurement results for 3 device types in 90nm and 40nm CMOS
  - High ESD protection achieved
- Plug-n-play approach demonstrated till 20 GHz
  - Excellent figures of merit
    - Low capacitance
    - Low leakage
    - High Q-factor
    - High ESD protection
    - Stable capacitance over voltage and frequency
  - Broad usability of silicon proven solutions

Outline

- Introduction
- ESD protection for advanced CMOS
- **ESD protection in high voltage, BCD**
  - **ESD protection in high voltage**
  - Automotive applications
- ESD protection in SOI technology
- Summary, conclusions

SOFICS
Solutions For ICs

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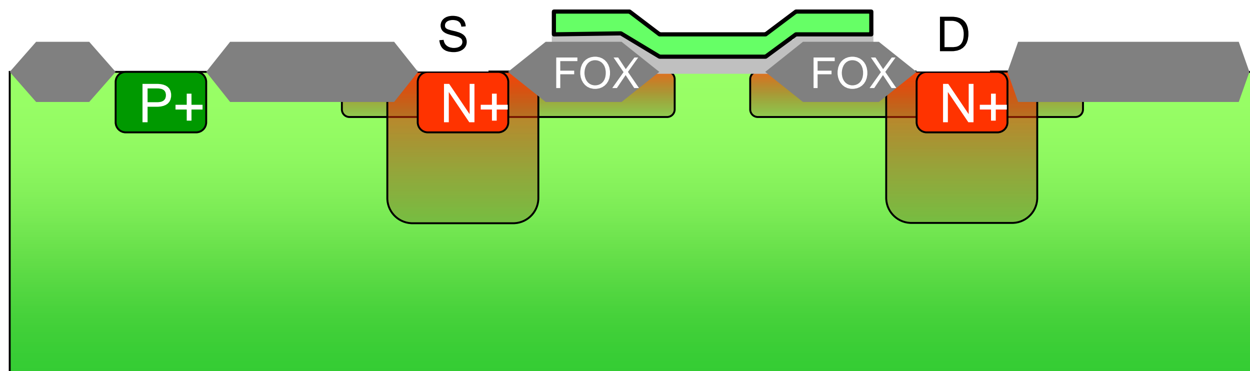
HV: fundamental differences

- **Thick gate** oxide for high voltage operation
- Drain, source gate **overlap using FOX or STI**
  - **Introduces defects at bird's beak or STI edges**
- **Low doping levels** to increase breakdown voltage
- **Large distances** to prevent punch-through

- Result: dramatic changes in ESD behavior

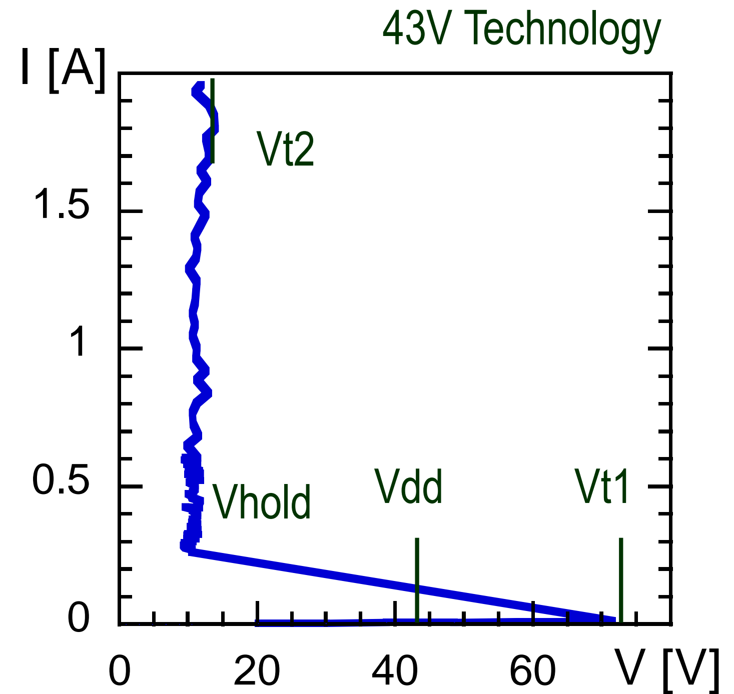


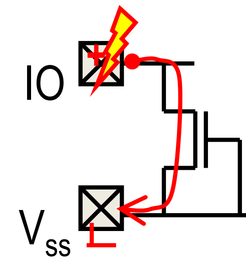
Strong snapback in HV-NMOS

- Large Vt1
- Very low Vhold, Vt2

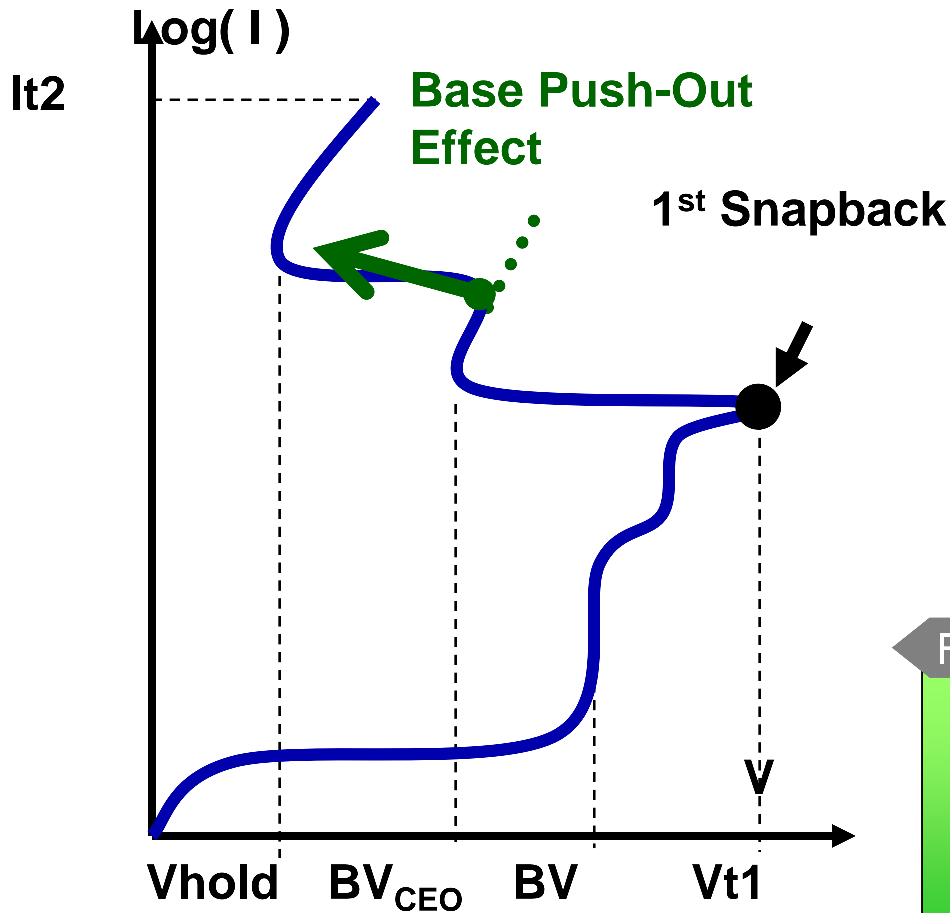
- Vt2 << Vt1
  - Multi-finger triggering very difficult
  - No ESD performance scaling!

- Vhold << Vdd
  - Latch-up risk
  - Not suitable for supply protection

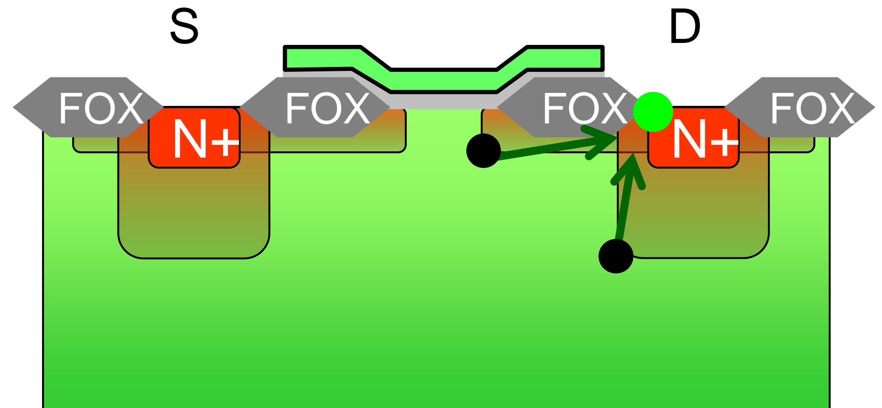




HV-NMOS in High injection

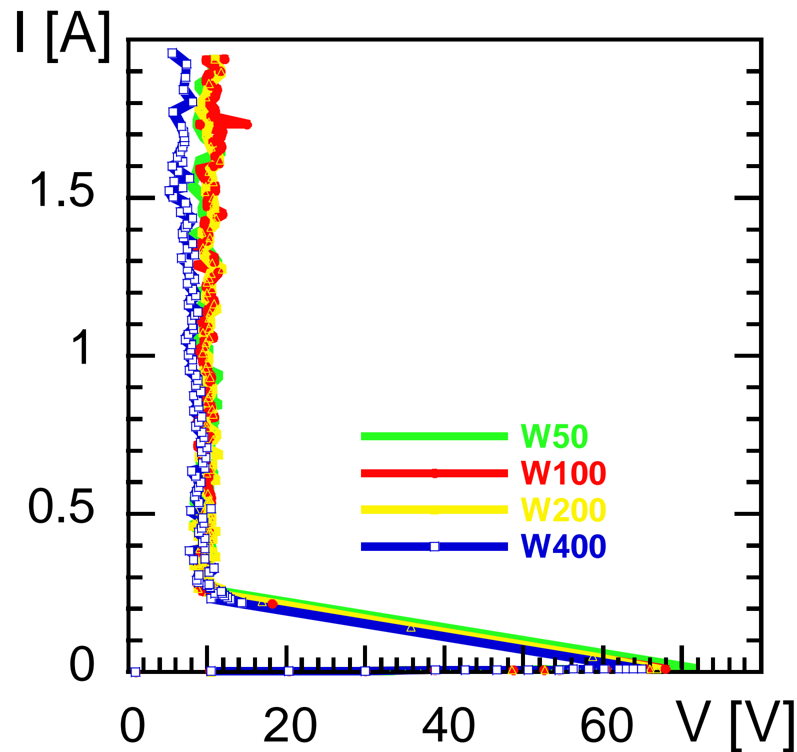


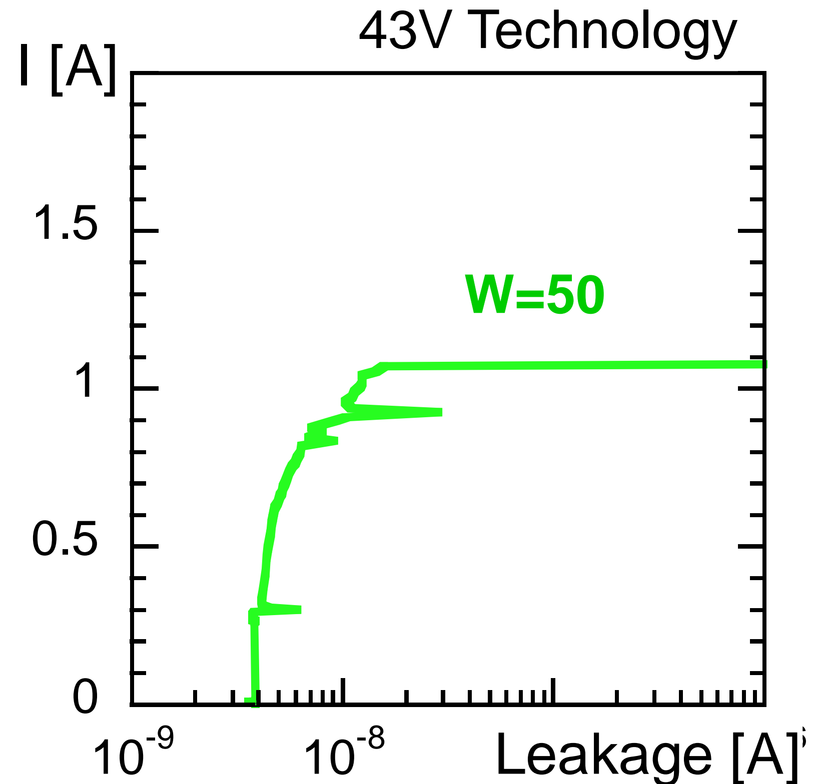
- Double snapback behaviour
  - Large BV, Vt1
  - Avalanche spot migration: Base push-out
  - Not always visible under TLP conditions



HV-NMOS: degradation at snapback

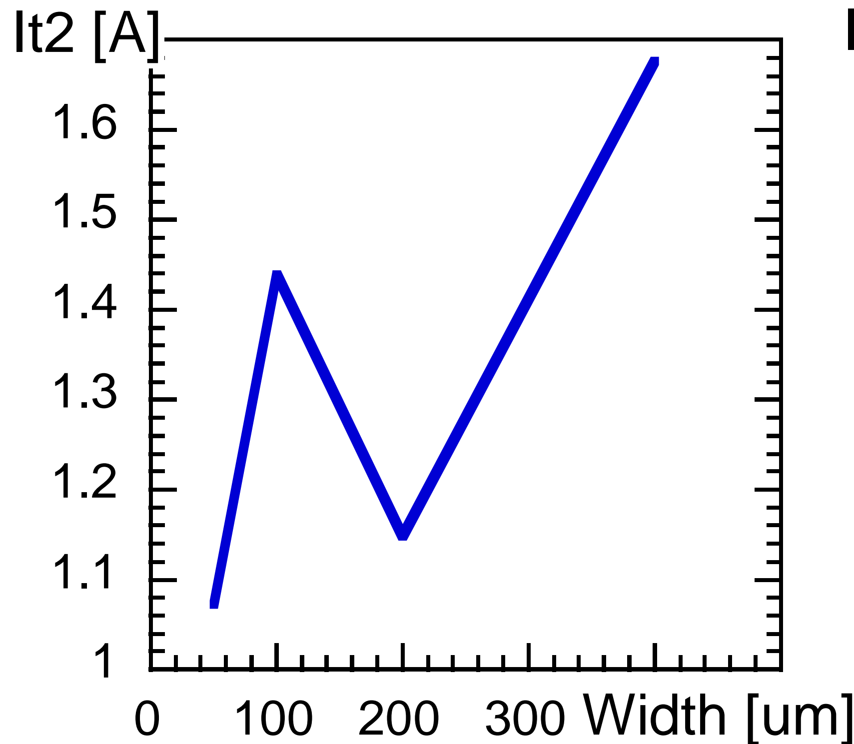
- **Slow increase of leakage current** is proof of degradation.

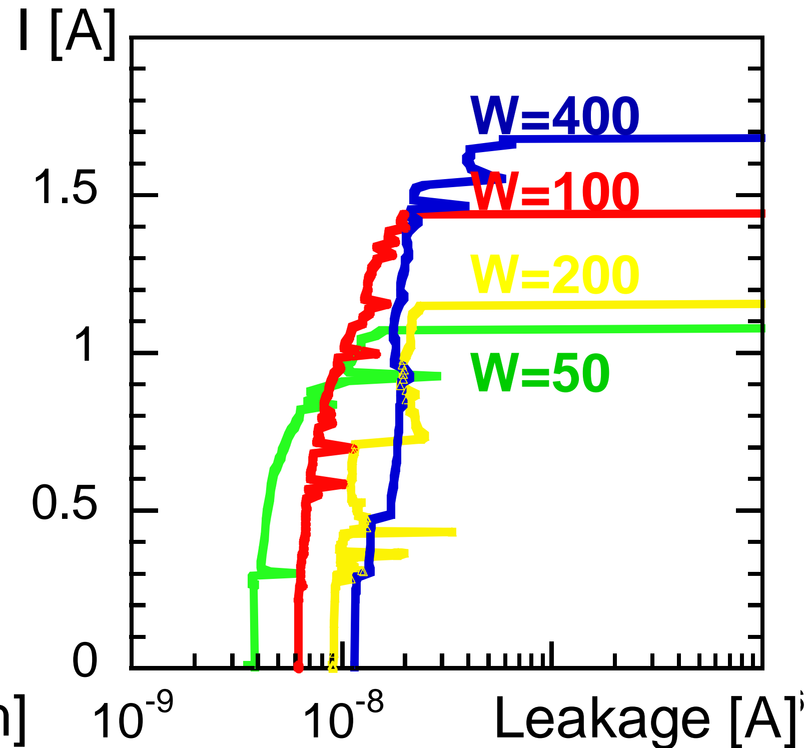




HV-NMOS: degradation at snapback

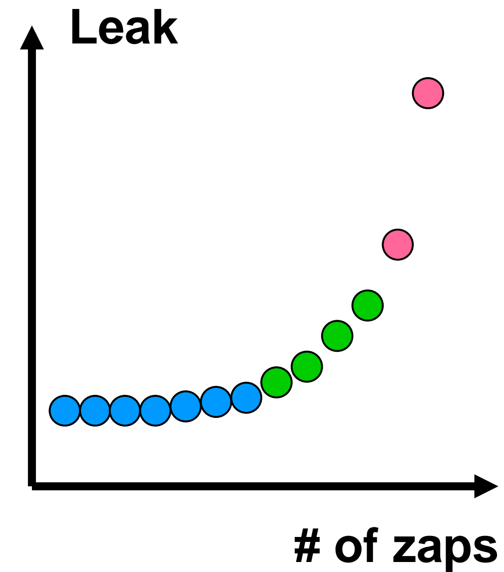
- Failure current It2 is not proportional to the total perimeter:
  - non uniform conduction in single finger structures

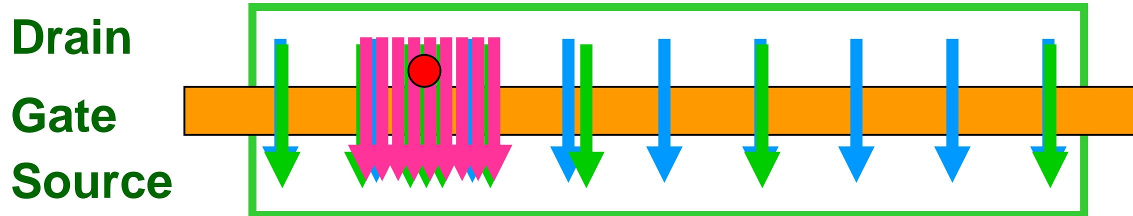


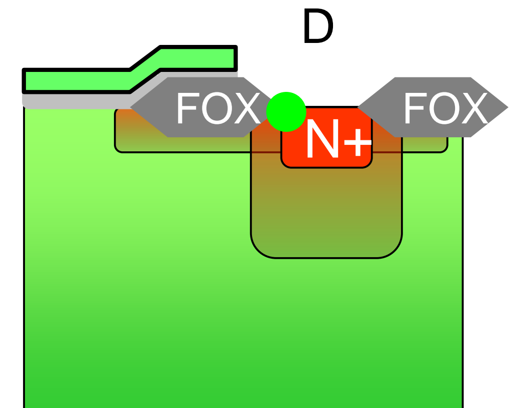


HV-NMOS: degradation at snapback

- Charge trapping at birds' beak
- Degradation
- Local Breakdown voltage reduction
- Non-uniformity during next stress

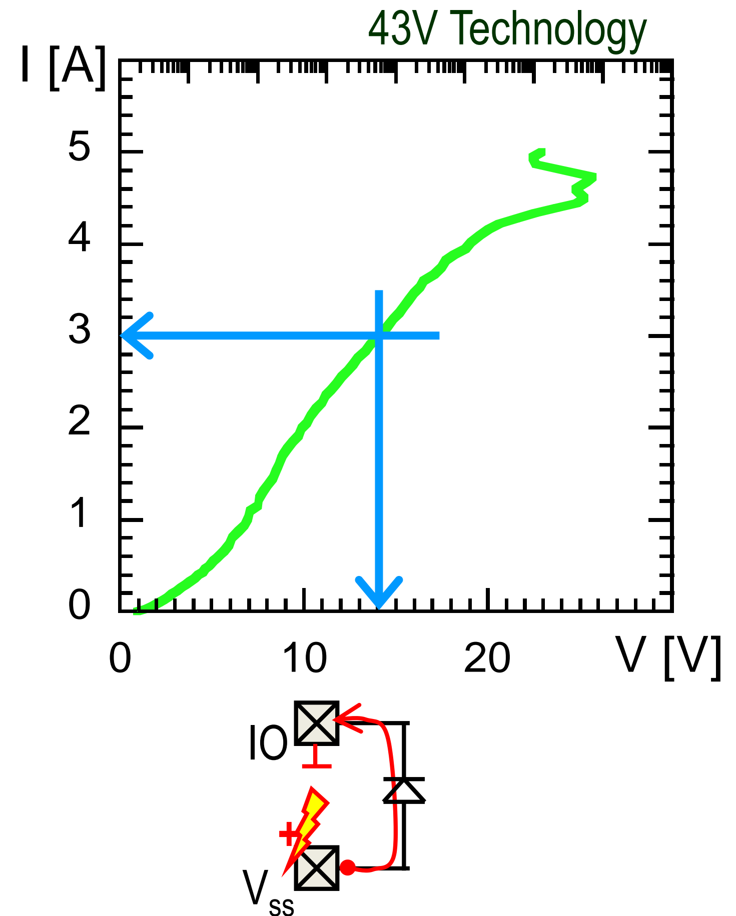






High resistive basic elements

- Resistive power busses
  - Limited number of metal layers
  - Applications with long bus lines
- Resistive diodes
  - Low doping levels
- Design margin penalty



HV ESD protection: challenges

- Parasitic NPN transistors in HV processes exhibit:
  - Strong snapback
    - High trigger voltage (Vt1)
    - Low holding voltage (Vhold) and failure voltage (Vt2)
  - Reliability degradation
    - Charge trapping due to Hot Carrier Injection
  - Non uniform conduction for ESD stress
    - In multi finger structures
    - In Single finger structures

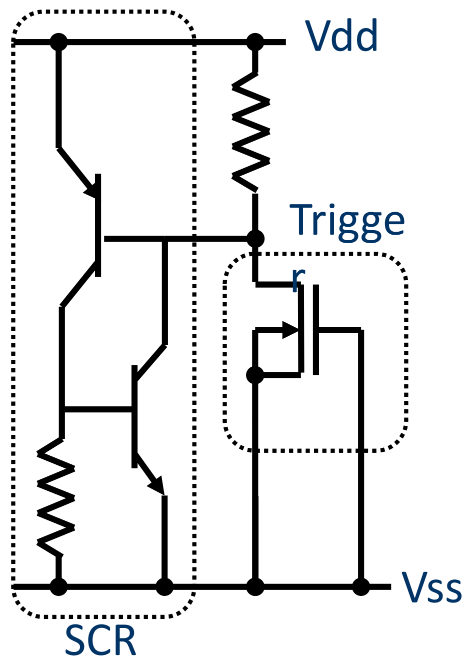
- High(er) resistance ESD discharge path
  - Due to low doping levels (diodes)
  - Due to limited number of metal layers

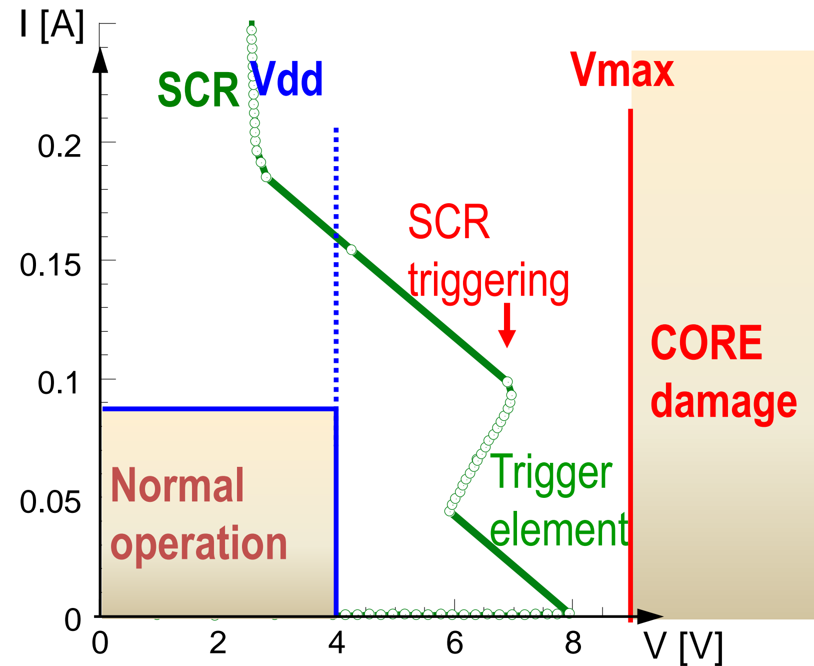
Power protection based on SCR's

- SCR's present a Latch-up danger during normal operation
  - The SCR holding voltage is below the Vdd operating voltage
  - SCR's remains latch-ed once triggered
  - SCR's can create a low ohmic path between Vdd and Vss
- **BUT**: prevention of Latch-up possible
  - Prevent SCR triggering during normal operation
    - Optimised design for high trigger current
    - Optimised SCR layout for high holding current

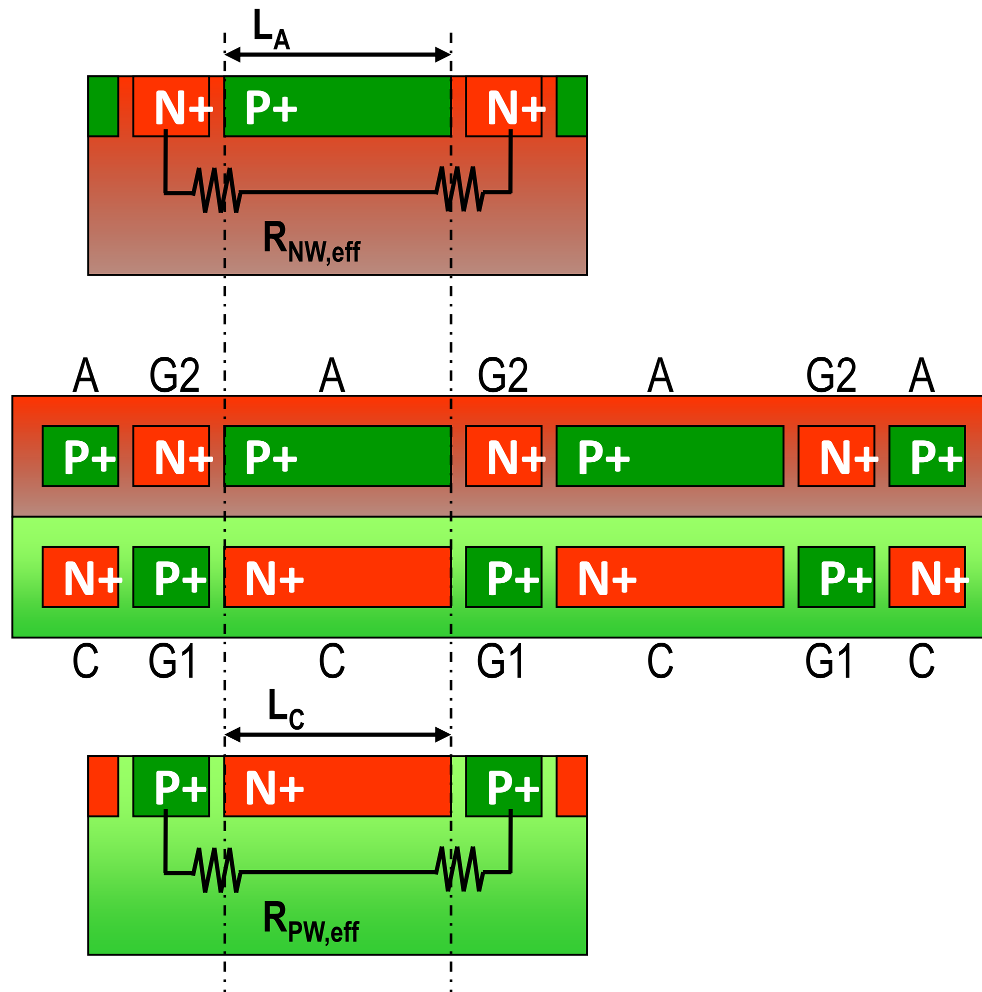
TakeCharge® SCR – Latch-up immune design

- Prevent SCR triggering during normal operation
  - Increase the trigger current through optimal trigger chain
  - Increase the holding current through SCR layout technique





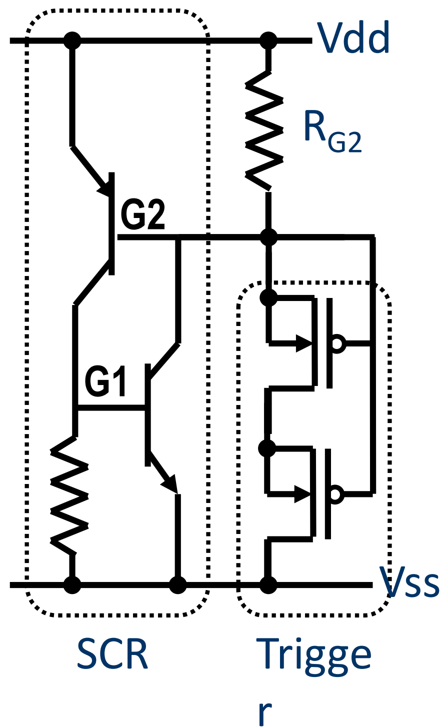
Segmentation layout technique



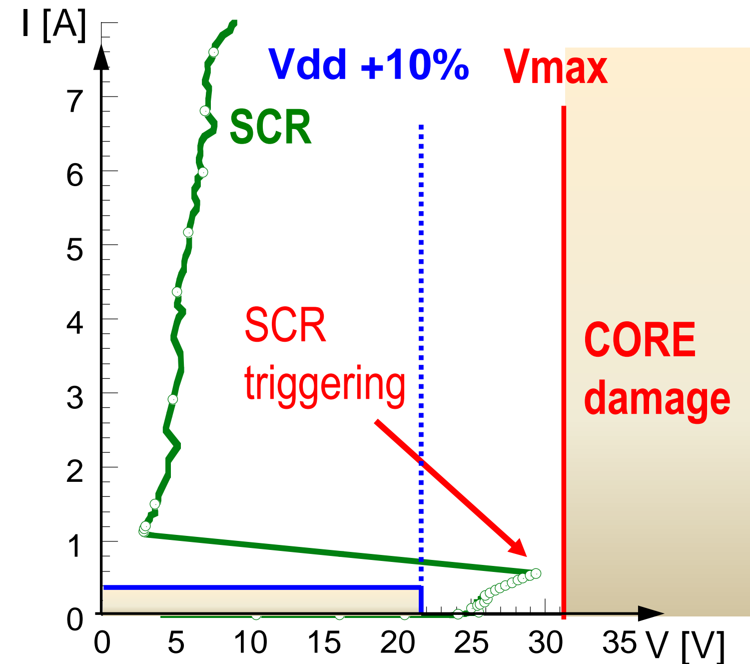
- Reduce effective well resistance
  - Segmentation of Anode and Cathode by N+ / P+ well ties
  - Reduced effective Anode and Cathode stripe lengths
  - Reduced effective well resistances below Anode and Cathode diffusions

TakeCharge® HV Power clamp example 2

- HV BiCMOS 22V – 0.5um
  - Tunable Latch free conduction level
  - Tunable trigger behavior independent of SCR
  - High SCR performance independent from trigger tuning



R_{G2} [Ohm]	It1 [mA]
1	565
2	275
5	118
10	60



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Outline

- Introduction
- ESD protection for advanced CMOS
- **ESD protection in high voltage, BCD**
  - ESD protection in high voltage
  - **Automotive applications**
- ESD protection in SOI technology
- Summary, conclusions

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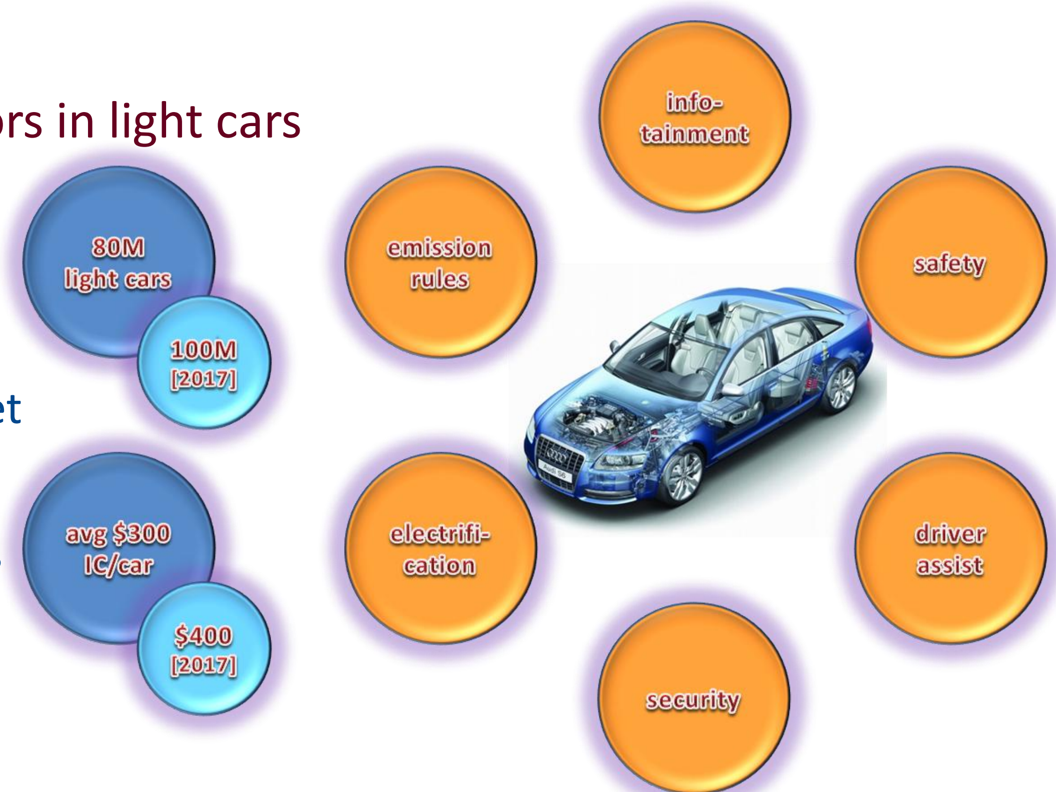
The automotive market

- Trend: more electronics in harsh EMI/EOS automotive environments
  - Electrification of systems
  - New regulations
  - New applications
- Trend: more semiconductors in light cars
  - $300 [2013]
  - $400 [2017]
- TAM:
  - $30B i.e. 10% semi market
- Reliability challenges:
  - Zero defect requirements
  - Very long system lifetime



Automotive electronics: not an “easy ride”

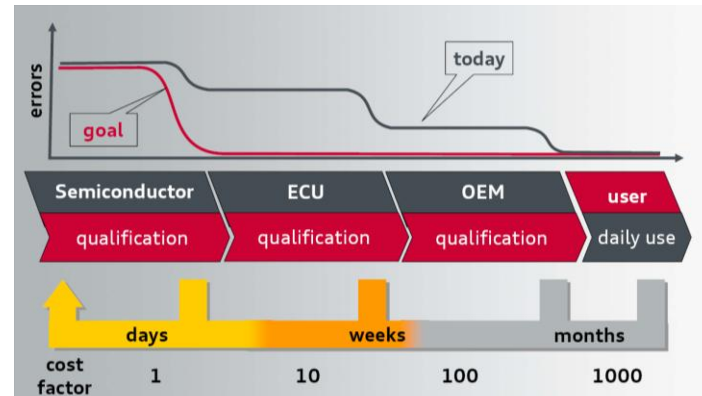
- Operation conditions different than consumer and industrial

	Consumer	Industrial	Automotive
Temperature	0 to 40°C	-10 to 70°C	-40 to 160°C
Operation time	2 to 5 years	5 to 10 years	up to 15 years
Humidity	low	environment	0% to 100%
Field failure rate	<10%	<<1%	0 failure
Supply	~ 1 year	~ 2 to 5 years	up to 30 years

- System (reliability) requirements are equally more stringent
  - DC: 12V, 24V, 40V…
  - Transient currents: several Amperes

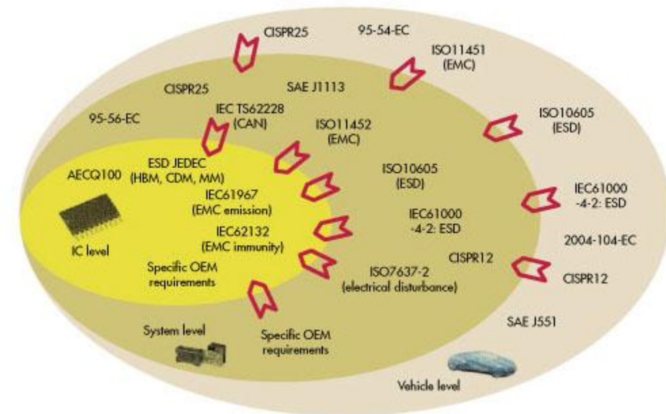
Automotive electronics: not an "easy ride"

- Zero defect requirements
  - Severe reliability tests and qualification
  - Cost of errors over product(ion) life time
    - *Early*-built-in reliability



Source: Audi, Christian Lippert

- Trend:
  - OEM push reliability specifications on the IC
    - Adds *complexity and cost* to the IC



Source: Freescale, David Lopez

Automotive electronics: not an “easy ride”

- Severe reliability requirements passed on component and system level
  - **Above standard** HBM, MM requirements
  - Transient **latch-up immune**
    - **-27V..+40V**
  - **ESD under powered conditions**
    - **0V..+18V**
  - IEC 61000-4-2 **system ESD**
  - ISO 7637-2 **load dump** pulse
  - **EMC** IEC 62132 **DPI**

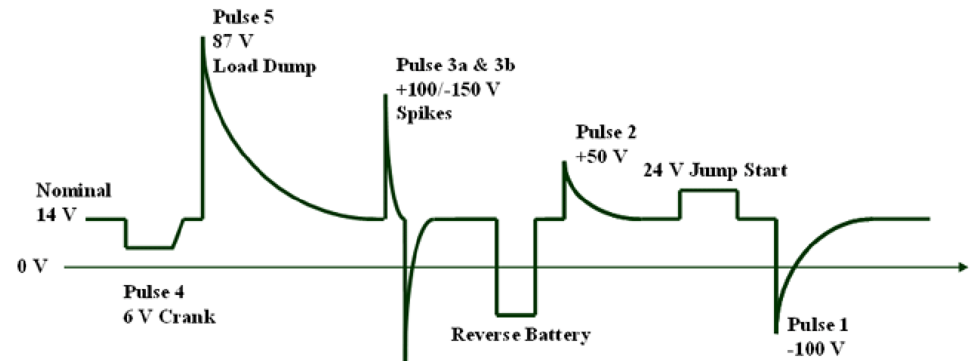


Figure 1: ISO7637-2 and main surges on automotive power rail

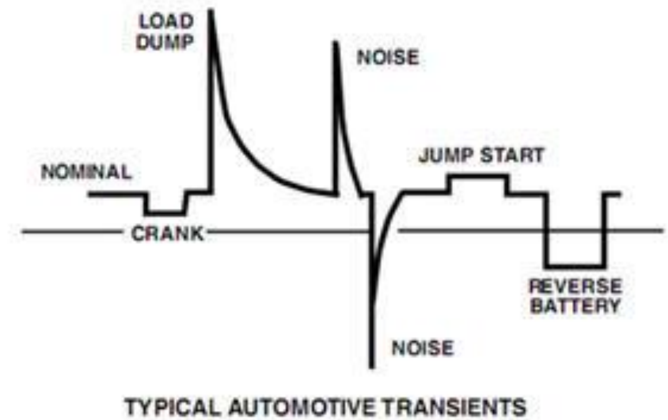
Source: STMicroelectronics, Philippe Merceron

- Requirements strongly depend on application
  - Automotive, industrial applications: IEC 61000-4-2, ISO 7637, IEC 62132 …
  - Battery, power management: IEC 61000-4-2

Automotive IC reliability design challenges

- **EOS**: Block DC current at high voltages
- **ESD**: Dissipate transient current, above (high) supply voltage
- **EMC**: Avoid false triggering

- Cost opportunity:
  - Reduce development time
  - Minimize on-chip protection area
  - Avoid dedicated process steps



Automotive LIN interface requirements

- Automotive LIN interface
  - Functional operation
    - 12V
  - Reliability considerations relevant for ESD
    - +/- 40V tolerant: bi-directional clamp required
    - 45V load dump (ISO 7637-2)
    - System level ESD robustness beyond 6kV IEC
    - EMC requirements
  - ESD clamp requirements
    - Trigger voltage, holding voltage > 45V
    - Transient latch-up safe
    - High ESD robustness > 20kV HBM
    - Tolerant against EMC

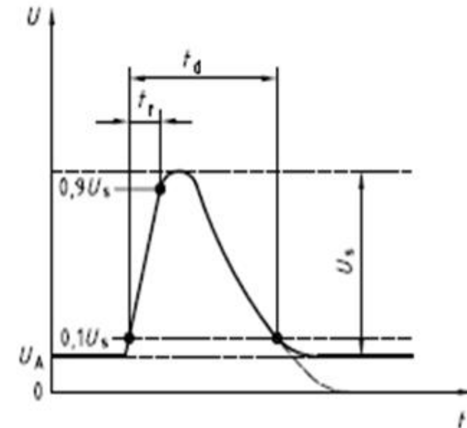


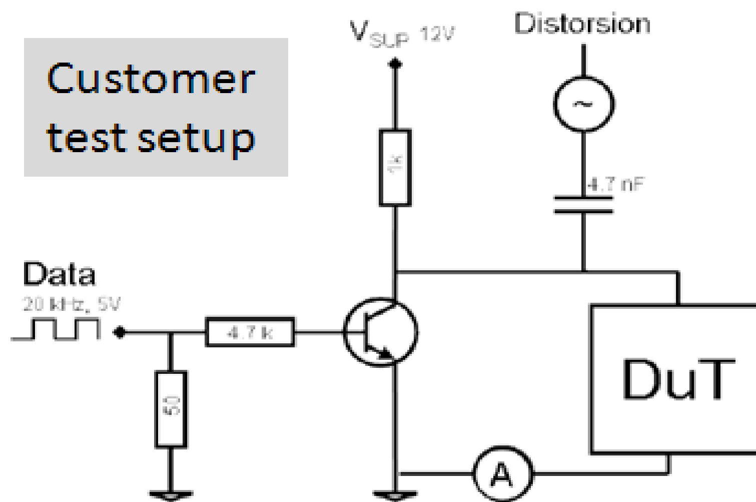
Figure 11 — Test pulse 5a

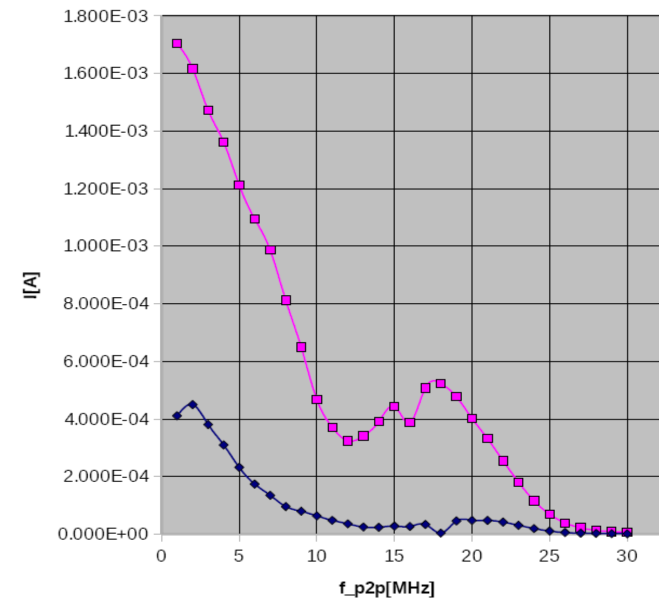
Table 9 — Parameters for test pulse 5a

Parameter	12 V system	24 V system
U_s	65 V to 87 V	123 V to 174 V
R_i	0,5 Ω to 4 Ω	1 Ω to 8 Ω
t_d	40 ms to 400 ms	100 ms to 350 ms
t_r	$\left(10 \,^{0}_{-5}\right)$ ms	

TSMC 0.25um BCD gen I – ESD solution for LIN

- Passing severe EMC specifications
  - Example: experienced IC maker for automotive applications
  - PowerQubic assessment for IEC 62132 DPI

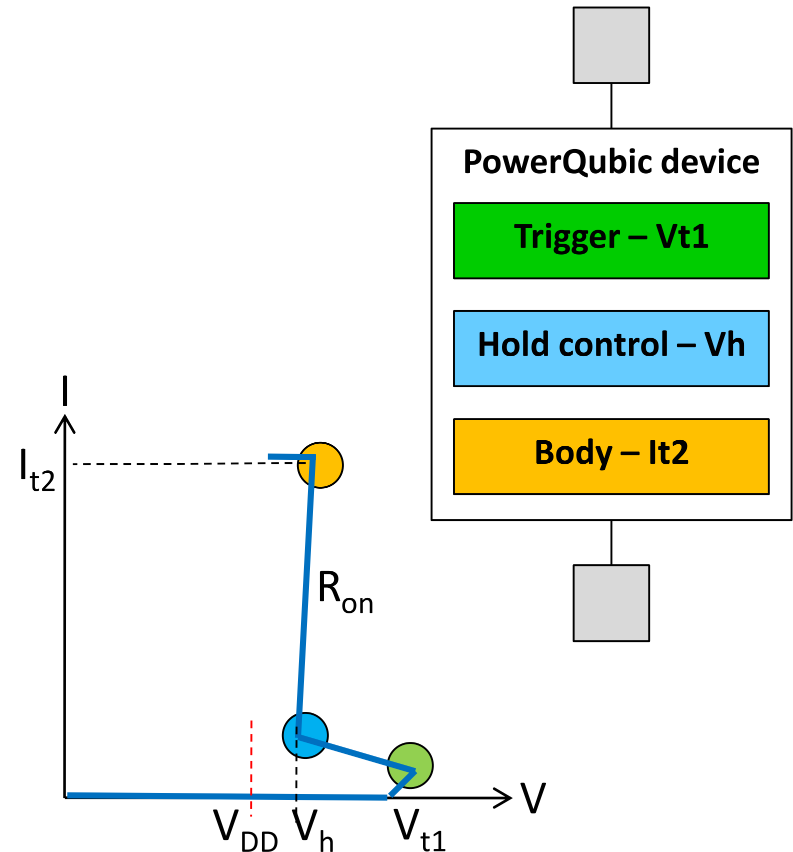




  - Result: Sofics PowerQubic devices tested
    "…better performance in EMC tests than the ESD structure we used so far"

Protect HV interfaces with Sofics' tunable clamps

- Tunable trigger voltage V_{t1}
  - External trigger circuit
    - Separate and interchangeable
    - Well established TakeCharge technique
- Tunable holding voltage V_{hold}
  - Holding circuit variations
    - By layout and/or design
    - Novel approaches
- Tunable performance I_{t2}, R_{on}
  - Clamp size variation
  - Different clamp bodies



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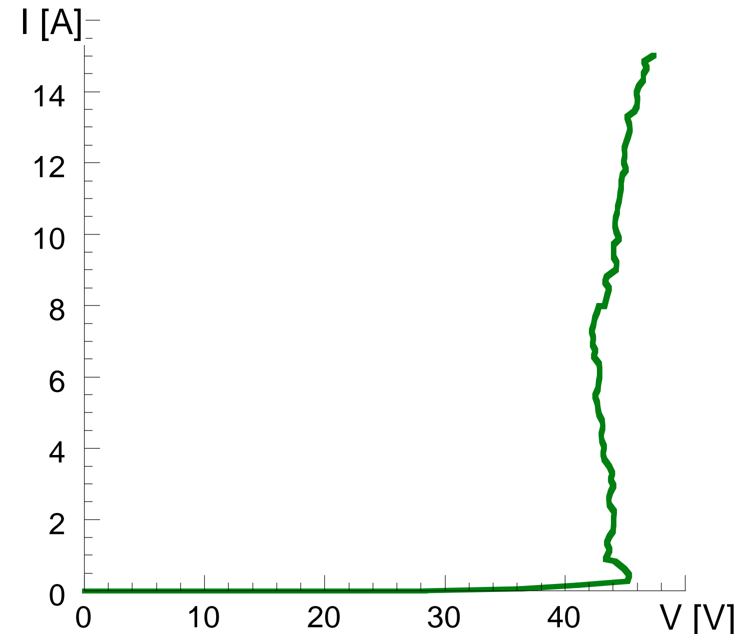
Sofics solution: PowerQubic clamp – example

- Automotive LIN interface protection clamp
  - High **ESD** performance
    - 16A TLP current (@ 48V)
    - 24kV HBM
    - 6kV IEC 61000-4-2 direct injection
  - **EOS** tolerant
    - Load dump pulse ISO 7637-2
    - Tolerant above 40V
  - Transient **Latch-up** immune
    - High holding voltage
    - At high temperature
    - For fast events



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  - **ESD challenges in SOI**
  - Solutions, concepts
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Challenges

- ESD Challenges in advanced SOI processes
  - Narrow design window for core protection
  - Extremely sensitive MOS devices
  - Sensitive thin gate oxide (GOX1)
  - Low robustness for basic ESD device such as diodes

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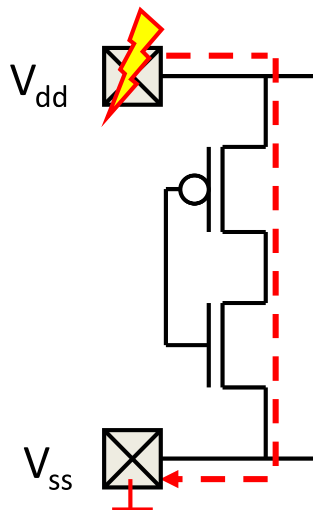
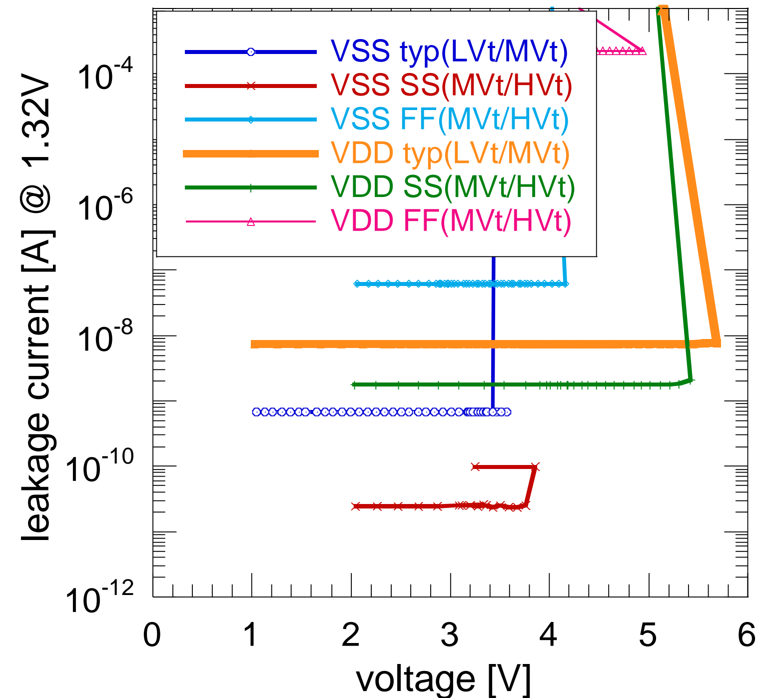
Low inverter breakdown voltage

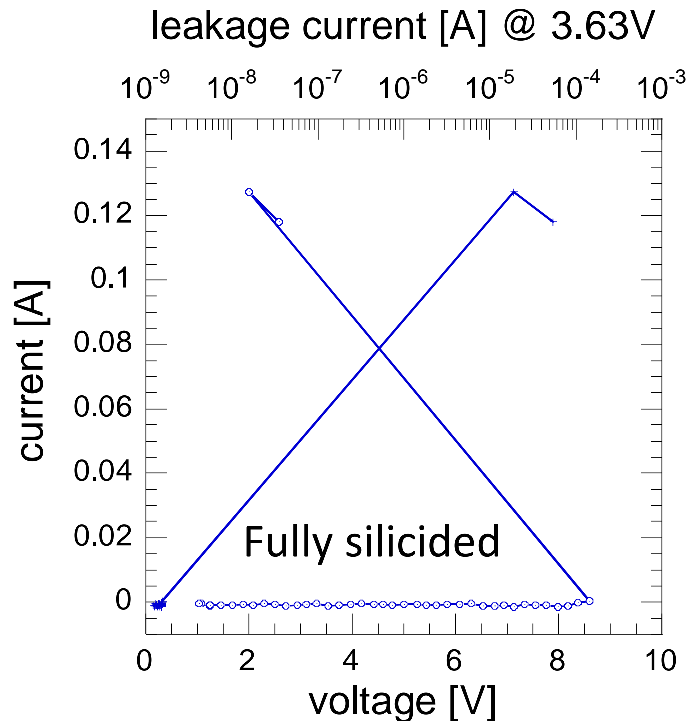
- Core breakdown measurements
  - Inverter structures tested on 90nm SOI process
  - Different gate connection options analyzed
  - Absolute Vmax ~3.6V

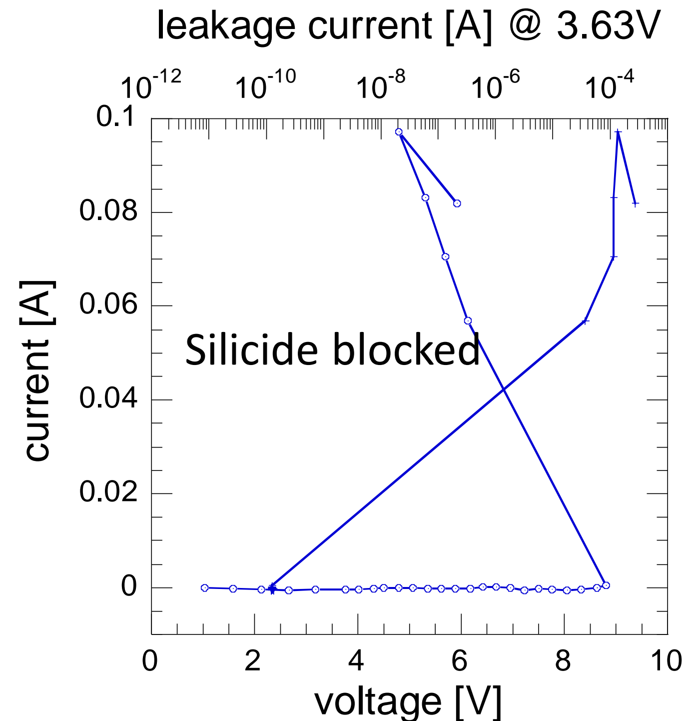




Sensitive MOS transistors

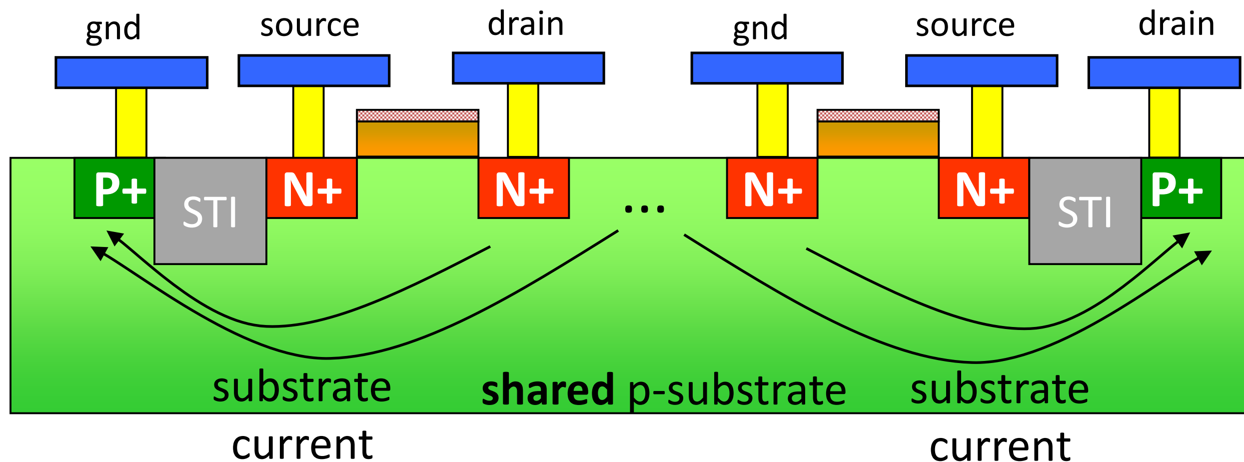
- GOX2 output drivers (NMOS)
  - Failure at snapback
  - Silicided or silicide blocked devices





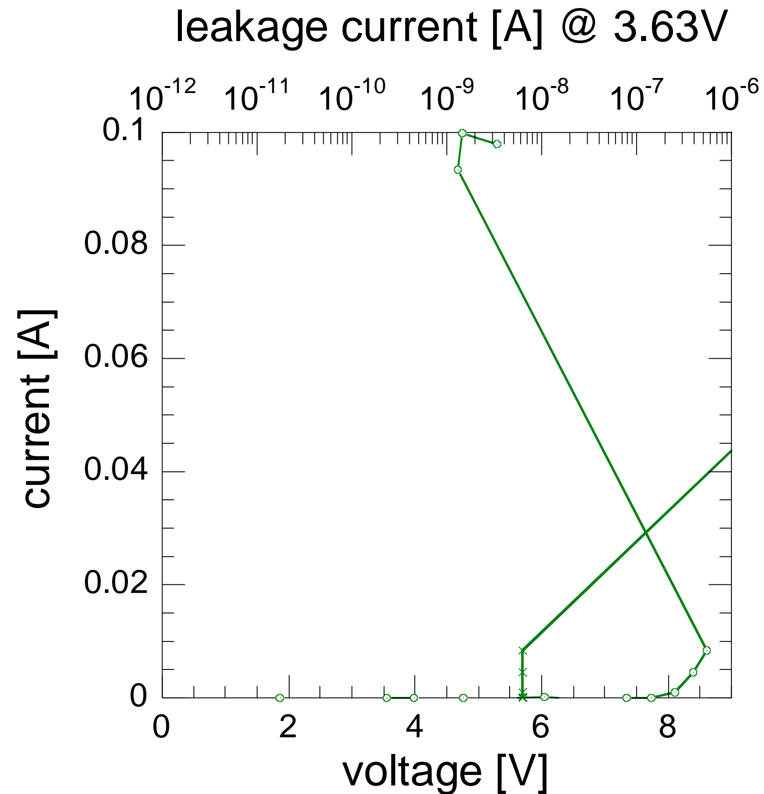
Background: NMOS in bulk technology

- NMOS in bulk technology has a shared P-substrate
  - Shared substrate helps to trigger all fingers
  - Vt1 of second/third/… finger is reduced due to biased bulk



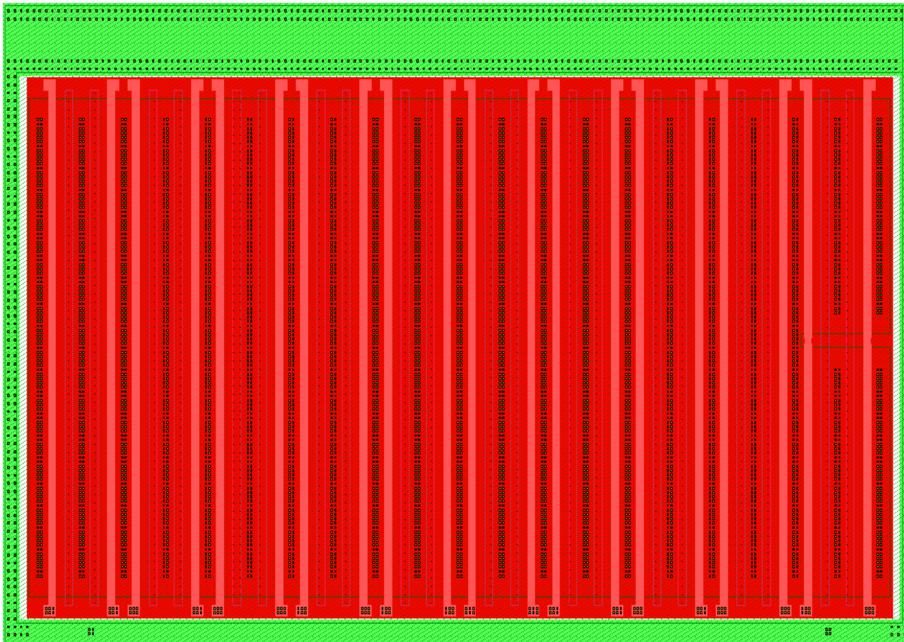
Background: Influence of the bulk resistance

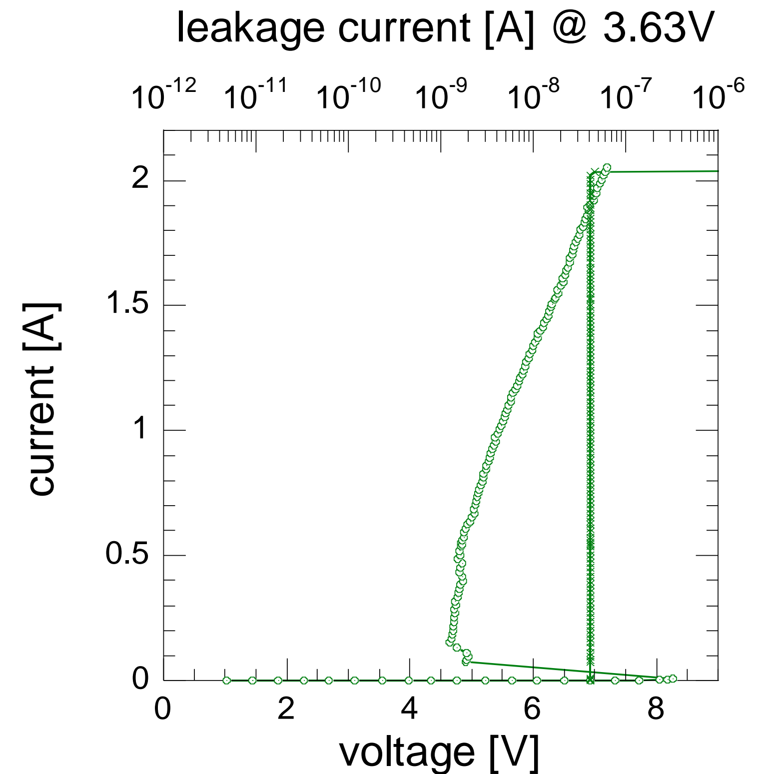
- Effect of effective substrate resistance on NMOS performance
  - Small size MOS fails at snapback
  - Guard-band too close to base region of parasitic NPN



Background: Influence of the bulk resistance

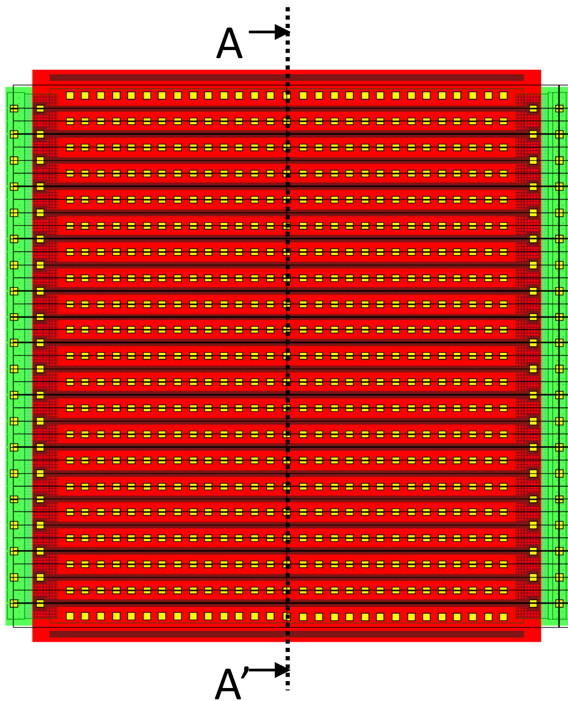
- Effect of effective substrate resistance on NMOS performance
  - Large size NMOS survives snapback
  - Effective substrate resistance in center of MOS is much higher

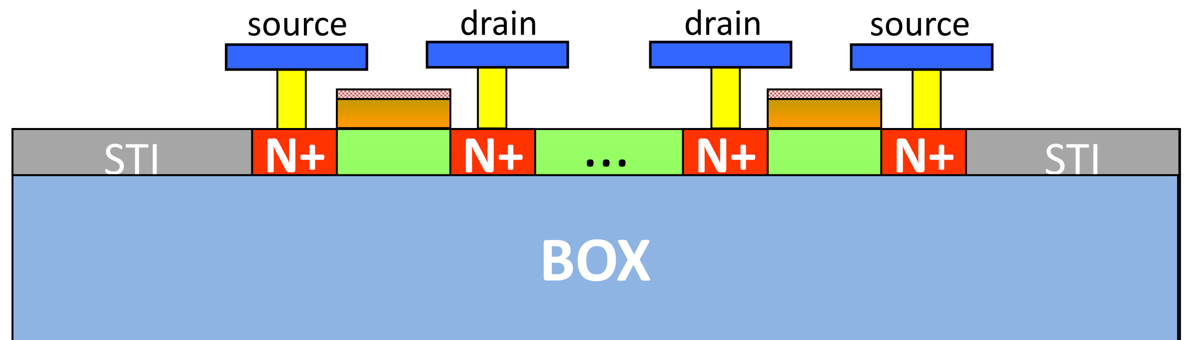




Background: SOI MOS has isolated body regions

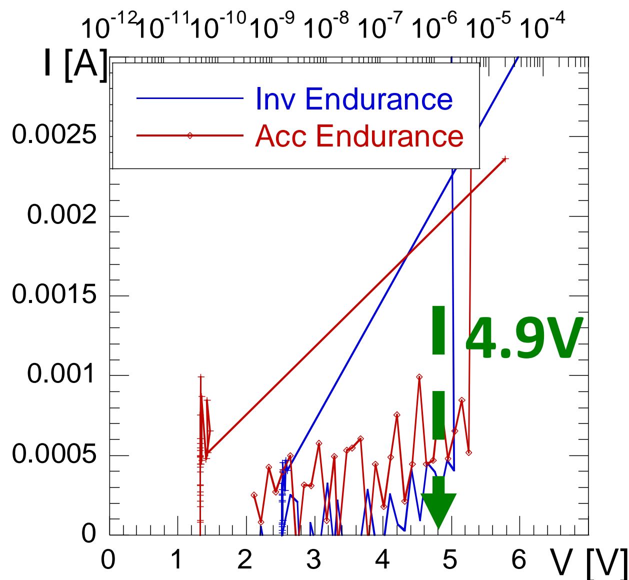
- Body regions are isolated
  - No body potential coupling between (adjacent) fingers

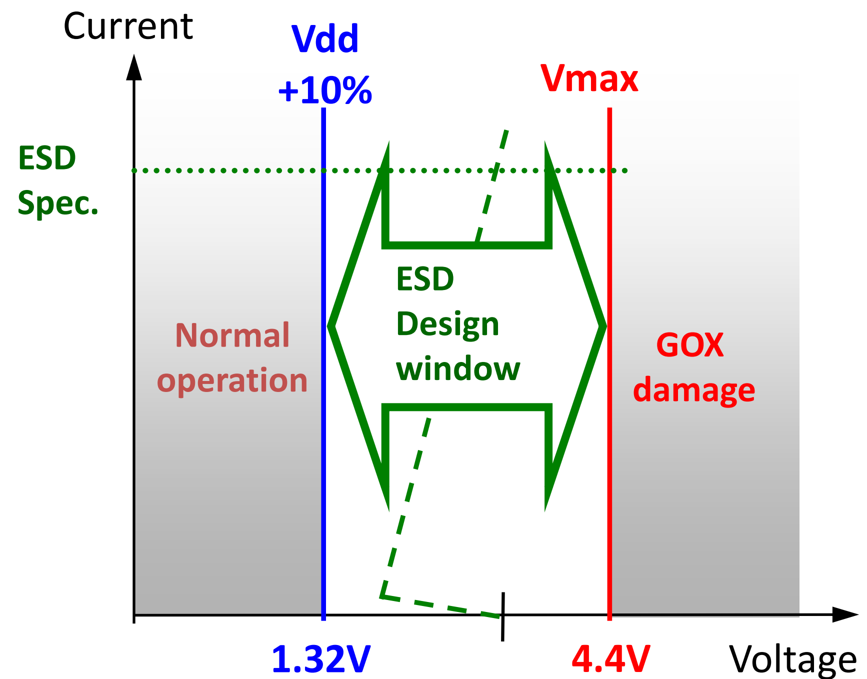




Narrow GOX1 design window

- Thin GOX gate oxide: low failure voltage
  - Analysis of maximum voltage during ESD stress
  - Endurance testing





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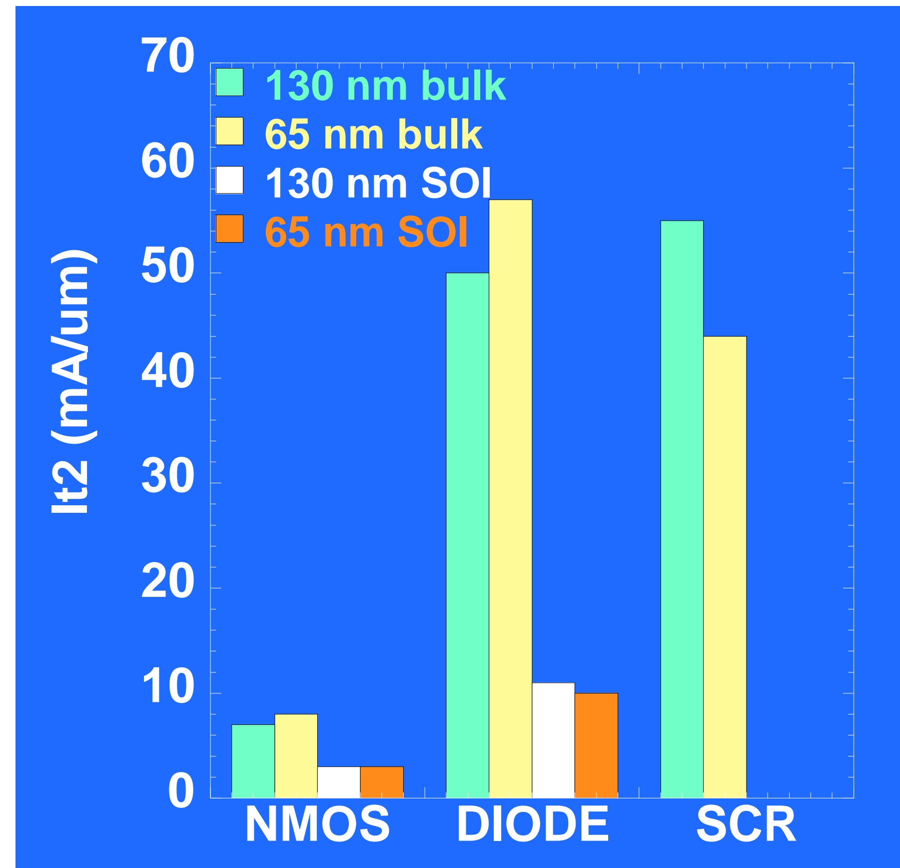
Low robustness for typical ESD devices

- SOI devices have low intrinsic failure current
- Typically $It2_{SOI}$ ~ $It2_{bulk}$ / 4
- Diodes have highest It2 in SOI

- Is it possible to create SCR's?



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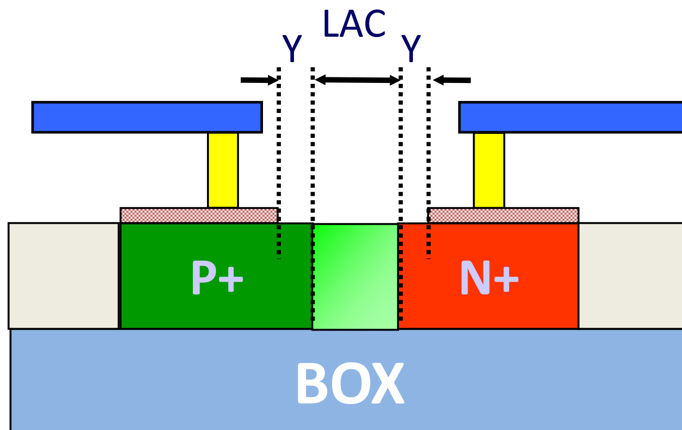
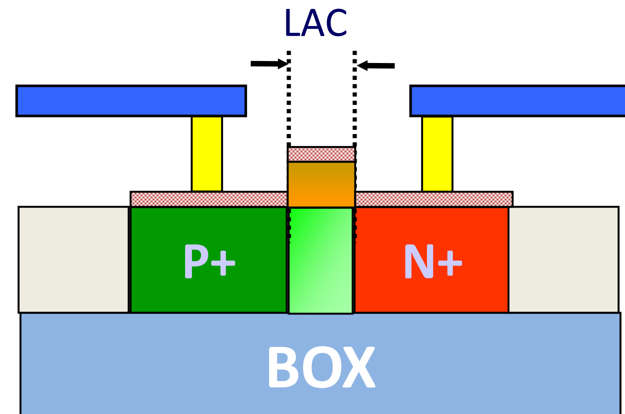
Analysis of diode structures

- Diodes
  - Basic building blocks for ESD protection
  - Required in almost all pin combinations
- Sofics' SOI analysis
  - Optimization of diode structure
    - Low capacitive
    - Small area
    - High ESD failure current
    - Low on-resistance
  - Different diode types studied
    - NO-STI diode
    - Gated diode

NO-STI vs. Gated diodes

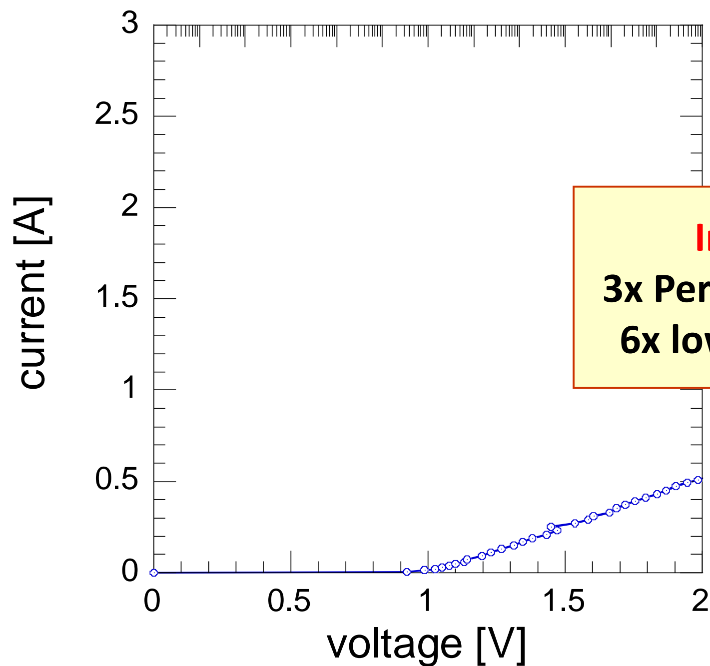
- NO-STI diode
  - **Larger LAC**: mask misalignment, depletion regions, out-diffusions
  - Y: mask-misalignment
  - **Higher series resistance**
  - **Relatively large in size**
- Gated diode
  - **Smaller LAC**: MDR gate length
  - **Oxide reliability** has to be watched
  - **Minimum resistance**
  - **Compact area**



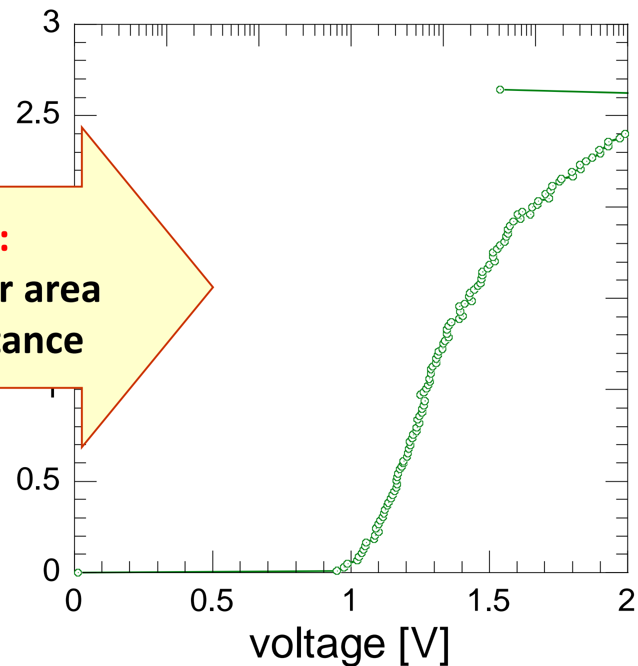


NO-STI vs. Gated diodes

- NO-STI diode
  - It2 per perimeter ~ 6.5mA/um
  - It2 per area ~ 3 mA/um²
- Gated diode
  - It2 per perimeter ~ 9.2 mA/um
  - It2 per area ~ 10.9 mA/um²



Improvement:
3x Performance per area
6x lower On resistance

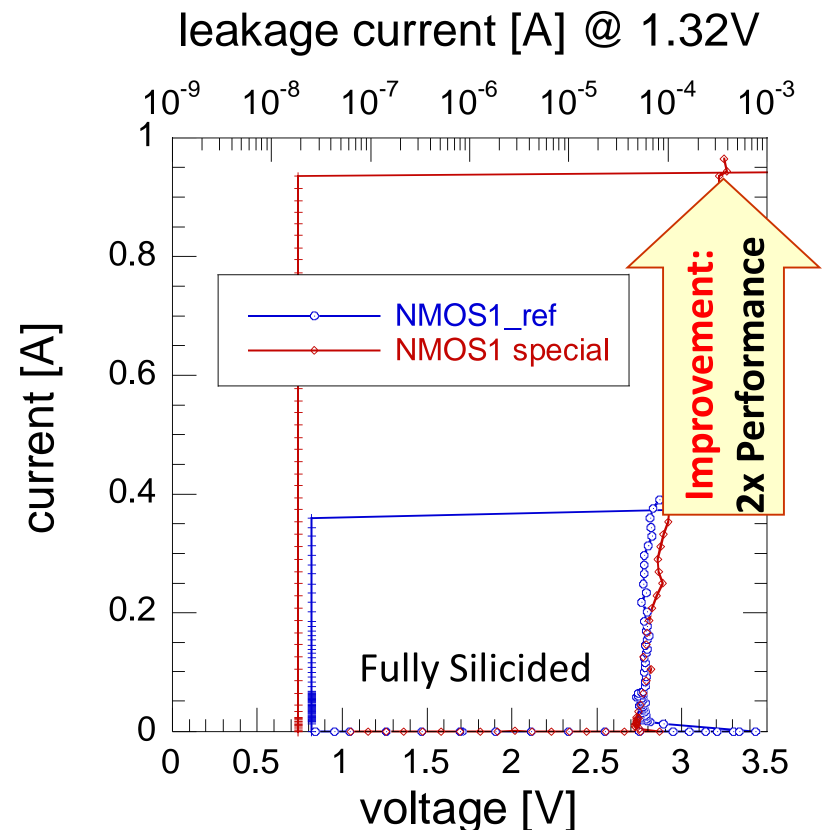


Analysis of MOS structures

- MOS
  - Self-protective output drivers
    - Maximize It2 per area
  - Non-self protective output drivers
    - Maximize design window (Vt2)
- Soifics' SOI analysis
  - Optimisation of MOS structure for ESD improvement
  - Investigation of failure voltage and current
    - Influence of silicide block
    - Influence of layout style
    - New layout approaches to boost performance

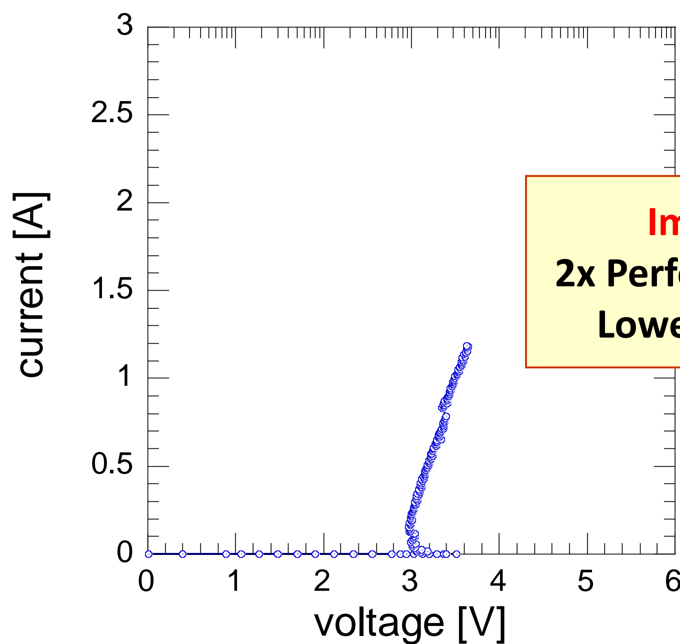
Performance improvement through layout

- ESD performance on 90 nm PD SOI
- Fully silicided 1.2V NMOS devices
  - Reference NMOS1
    - Standard fully silicided MOS driver
    - **Low performance (0.75 mA/um)**
    - **Large statistical variation**
  - NMOS1-special layout
    - Proprietary layout technique
    - **Much higher performance (1.58 mA/um)**

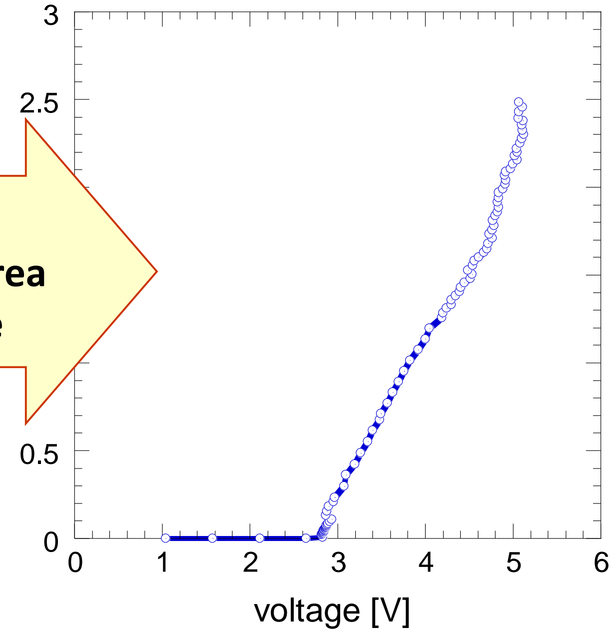


MOS performance improvement options

- Traditional solution
  - Silicide blocked drain junction
  - Optimal DCGS = 1um
- Sofics approach
  - Proprietary layout technique
  - Lower Vt1
    - Uniform triggering



Improvement:
2x Performance per area
Lower on resistance



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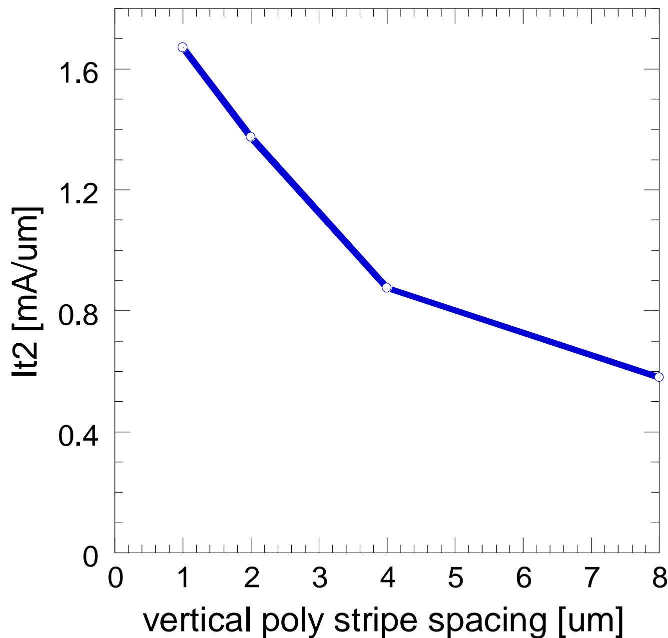
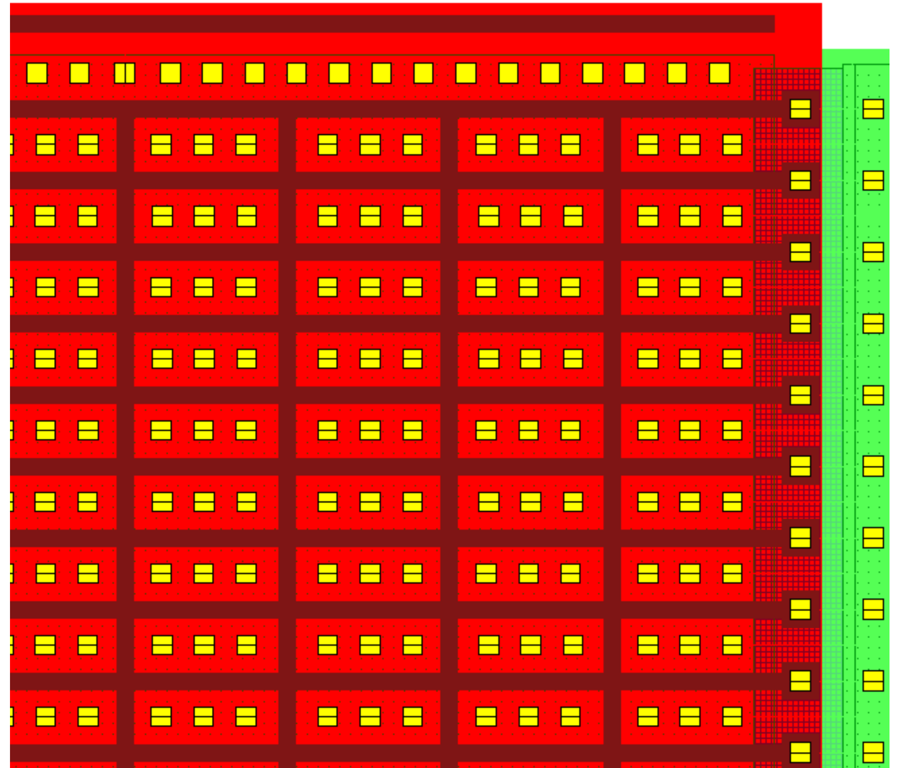
GOX 1 FS NMOS – improved body coupling

- No body coupling in PD SOI process
  - Special layout technique: Vertical poly stripes enable body coupling in PD SOI
  - Performance significantly improved
    - Vt2>Vt1 not necessary anymore





SOI MOS – Lower intrinsic current capability

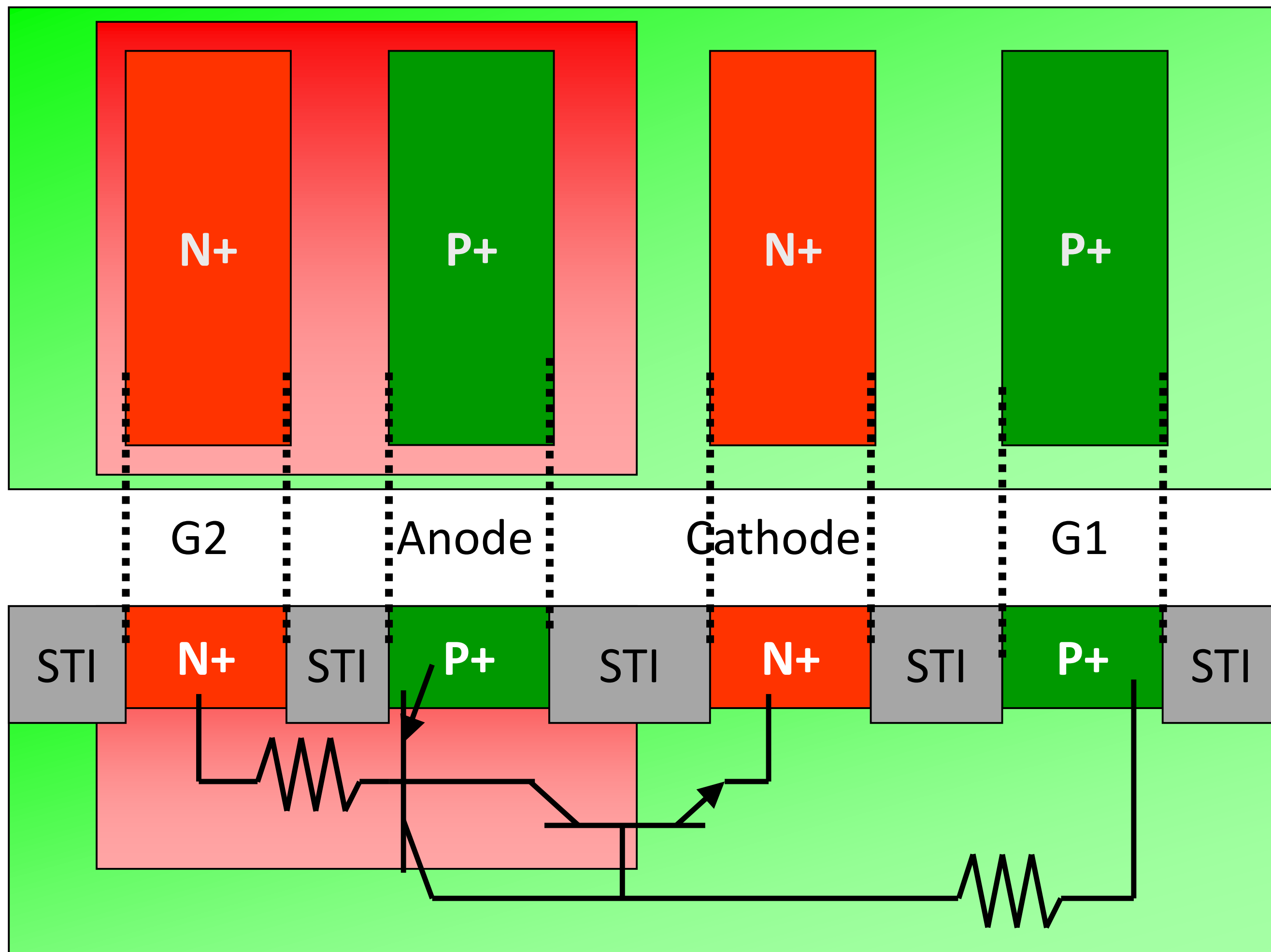
- high thermal resistance of buried oxide layer
  - SOI has lower intrinsic current capability
- Ballasting is often used to increase the maximum voltage across device
  - Make Vt2 > Vt1 to make sure all fingers trigger
  - Increase maximum voltage across output buffer
    - Increase design window for dual diode protection
  - Ballasting less effective for SOI due to reduced intrinsic current capability
    - Example: voltage across 5 ohm resistance, W = 100 um
    - Bulk process:
      - It2 ~ 9 mA/um (typical value)

      >> Voltage across resistor: 900 mA x 5 Ohm = 4.5V
    - SOI process
      - It2 ~ 2 mA/um (typical value)

      >> Voltage across resistor: 200 mA x 5 Ohm = 1V

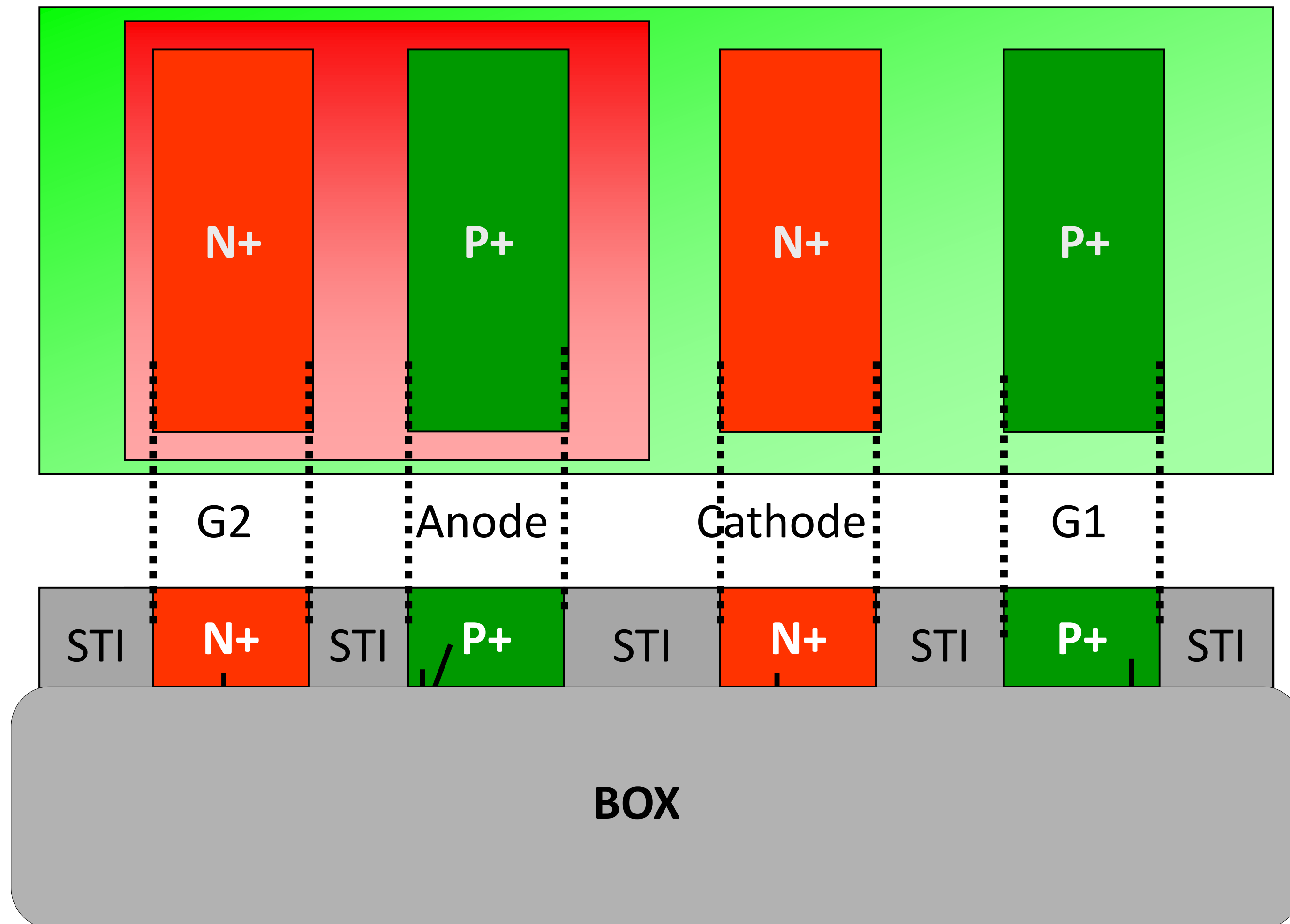
Is it possible to design SCRs in SOI?

- Basic SCR structure in Bulk technology



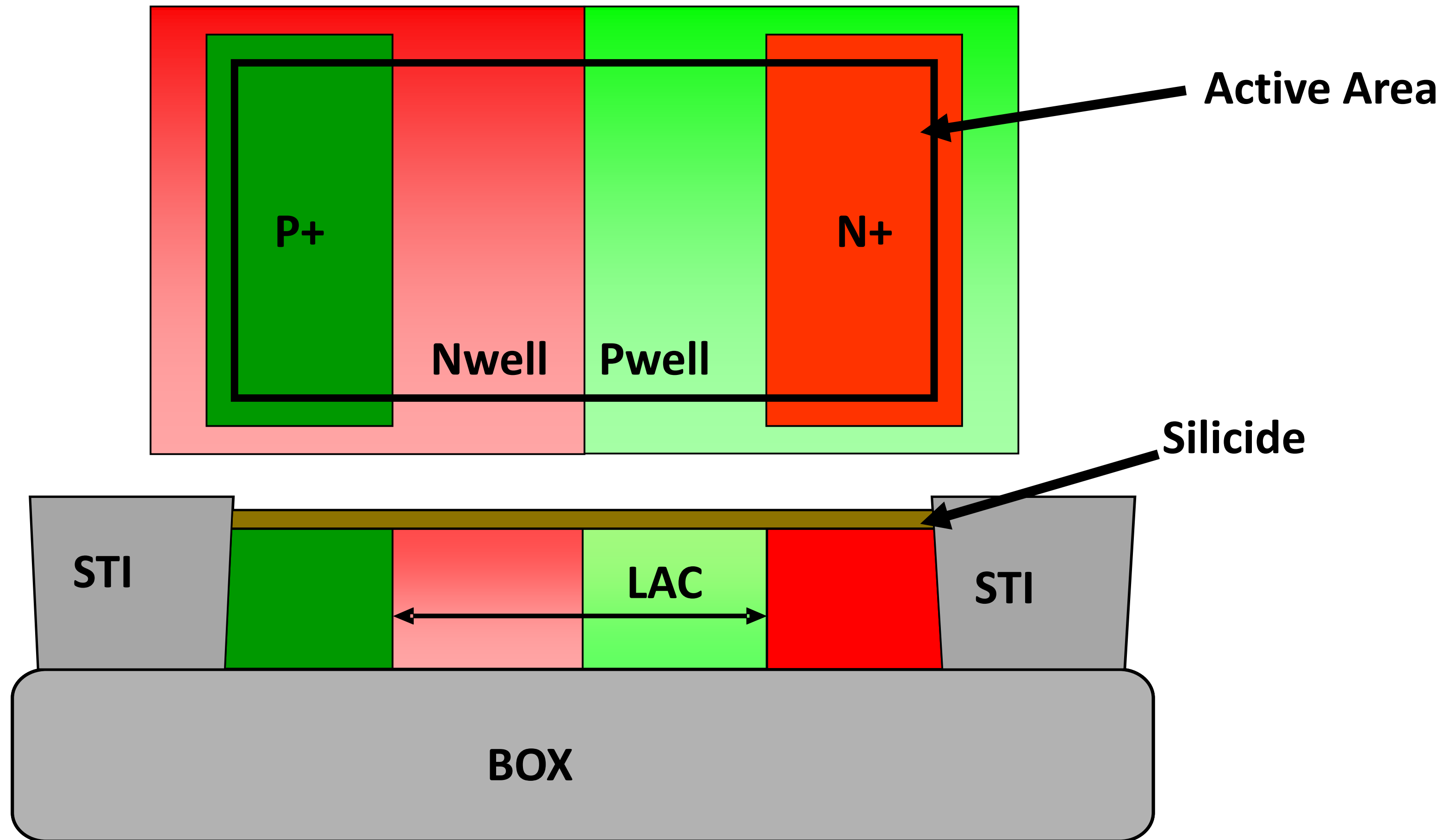
Is it possible to design SCRs in SOI?

- Basic SCR structure in SOI technology



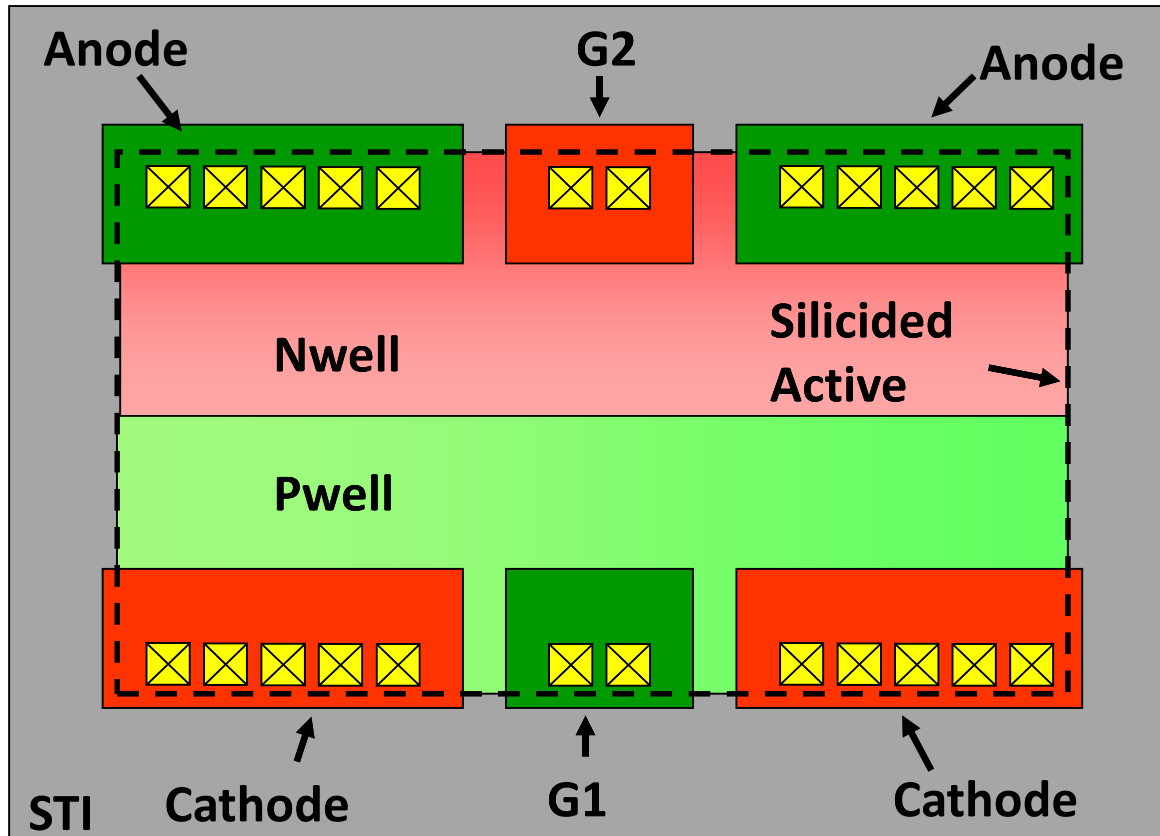
Constructing SCR in SOI (1/3)

- Step 1: remove STI between junctions – create active area without implant



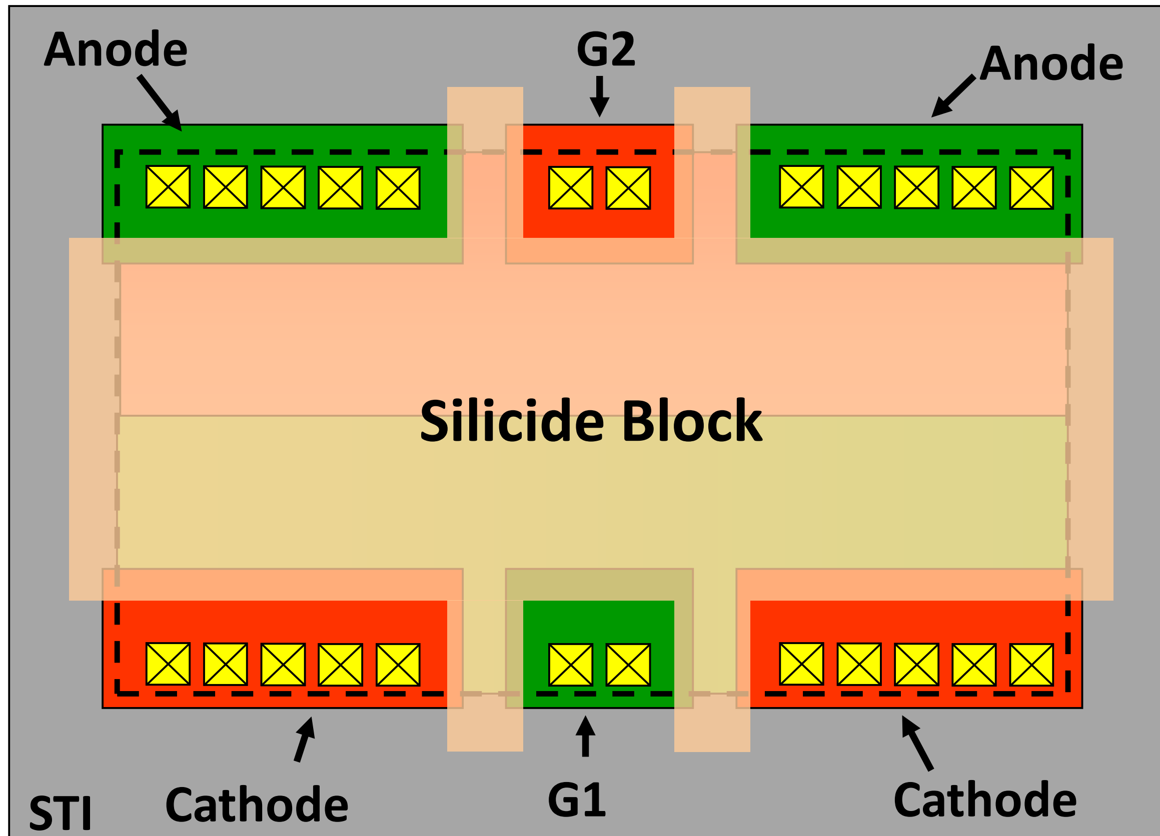
Constructing SCR in SOI (2/3)

- Step 2: Create G1/G2 – Segmented layout style



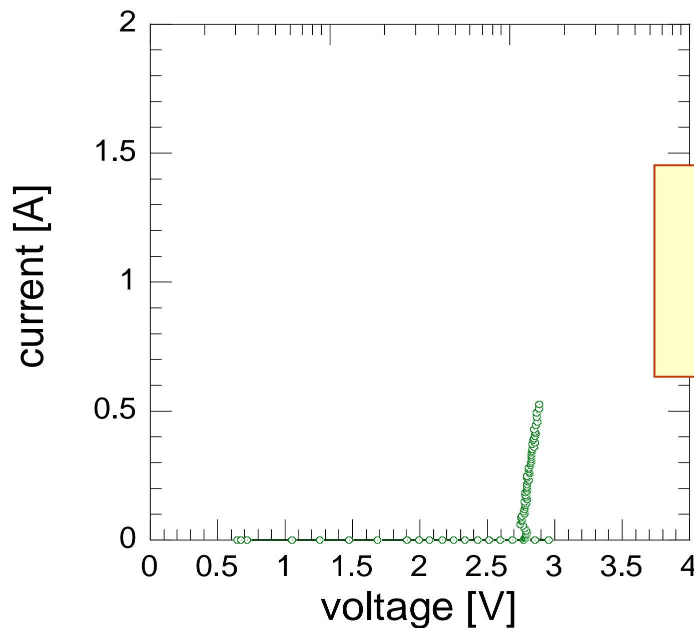
Constructing SCR in SOI (3/3)

- Step 3: Isolate regions – Apply Silicide block pattern

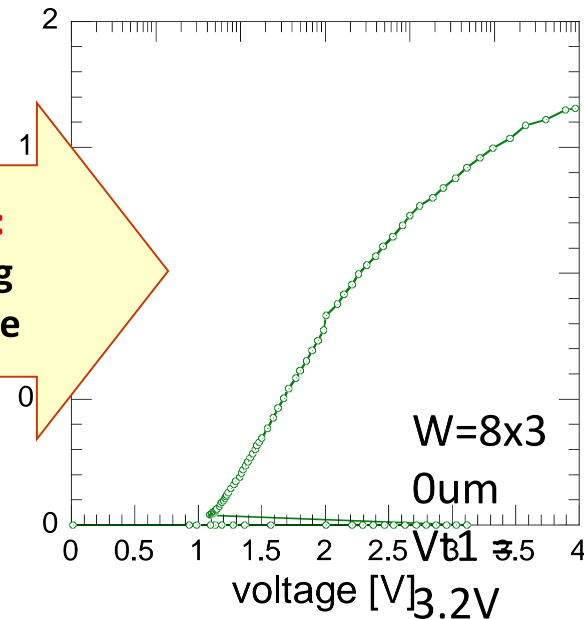


Ultra low voltage clamping through SCR's

- GOX1 NMOS
  - Holding voltage = 2.8V
- DT-SCR
  - Holding voltage of 1V
  - Extra margin for voltage drop over bus resistance



Improvement:
Lower clamping voltage possible



Conclusion

- Many **challenges** for ESD protection in SOI process
  - Narrow design window for core protection
  - Extremely sensitive MOS devices
  - Sensitive thin gate oxide (GOX1)
  - Low robustness, high Ron for standard ESD diodes

- **TakeCharge**® solutions
  - Diode improvement: larger performance per area
  - Various MOS robustness improvements
  - Low voltage clamping with Silicon Controlled Rectifiers (SCR)

Sofics experience on SOI

- Sofics experience in SOI applications

Application	CMOS node
High performance computing	90nm (PD) – 65nm (PD)
Computing platform feasibility study	90nm (BST)
General digital, analog and high temperature	130nm (PD) STM
High temperature, High voltage	1um XFAB

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Outline

- Introduction
- ESD protection for advanced CMOS
- ESD protection in high voltage, BCD
- ESD protection in SOI technology
- **Summary, conclusions**
  - **Summary**
  - **Trends**
  - **Tools**
  - **Conclusions**

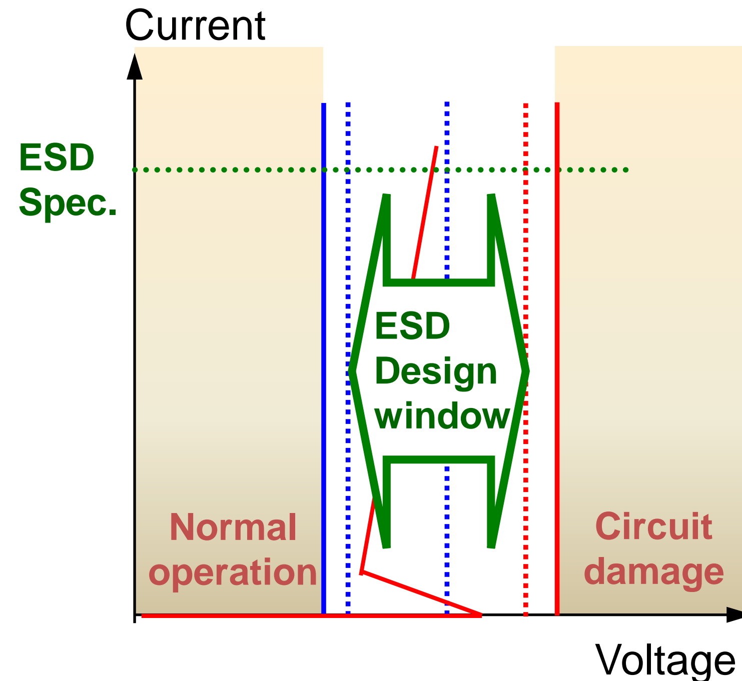
SOFICS
SOLUTIONS FOR ICs

Conclusions

- ESD designs requires mix of Circuit/device understanding
- Often devices are used beyond their Normal Operation use
  - Processes are not optimized for ESD use
  - Need to understand the device physics
- New technologies poses severe problems:
  - Critical voltages are reduced
  - SOI/FinFETS: Thin film reduces current capabilities
- New applications limit useable solution space
  - Low Capicitance solutions and matching needed
  - SOC gives higher complexity

How to deal with ESD? - Design window

- Summary of the requirements for ESD protection switches.
  - Invisible during normal operation
    - Low leakage
    - Low capacitance (speed!)
    - No latch-up (LU) issues
  - Protecting during ESD
    - Robustness: Large current shunting capability
    - Effectiveness: clamping voltage to safe value



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Overview of ESD clamp devices

- Snapback Clamps
  - Avalanching junctions trigger clamp
    - Process tuning required: Avalanche voltage can shift
    - Trigger voltage can be high
    - Multiple clamps along power buses do not work well in parallel.
    - Examples: Snapback ggNMOS, LVTSCR, GG-SCR
  - Triggering without avalanche
    - Easy portable between process nodes
    - Trigger voltage tuning by
      - Diode strings, Active MOS elements, power-up state detection
    - Examples: DT-SCR, RC-SCR, ESD-on-SCR

Overview of ESD clamp devices

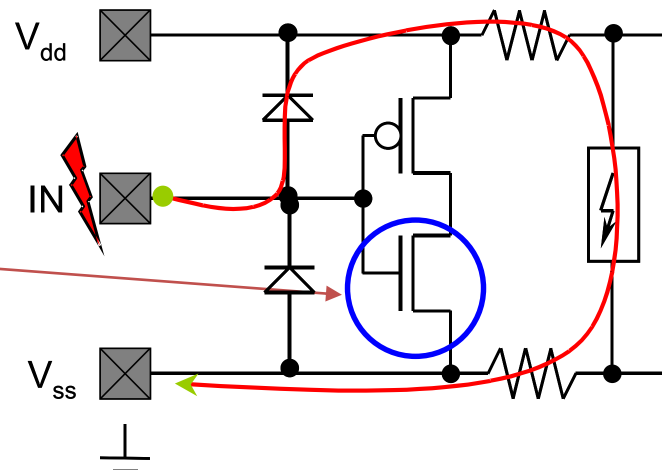
- Non-Snapback Clamps
  - Active MOSFET clamps
    - MOS action only
    - Very large width for low R clamp
    - Trigger circuit required
    - Examples: BIGFET approach
  - Diode Strings
    - String length sets stand-off voltage
    - Leakage at temperature can be a concern

Summary: Two failure modes during ESD

- Robustness of one of the ESD elements is too low
  - One or more elements in discharge path can't handle the ESD current
- Non-effective protection
  - Total voltage drop over the protection elements is too large
  - Critical element can't handle this voltage

Example:

Critical element = gate oxide of NMOS



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Summary: ESD calculations

- Investigate the stress cases one by one
- Step 1
  - Define the sensitive elements
    - Gate oxides, small MOS devices, core elements, resistances
  - Define the Maximum voltage for these elements
    - Select the worst case = Vmax
    - Use a safety margin
- Step 2
  - Create a safe ESD shunt path
    - Robust elements
  - Calculate the total voltage drop over the ESD path = $V_{ESD\text{-}PATH}$
- Step 3: Check: $V_{ESD\text{-}PATH} < Vmax$?

Outline

- Introduction
- ESD protection for advanced CMOS
- ESD protection in high voltage, BCD
- ESD protection in SOI technologies
- Summary, conclusions
- **Sofics' business approach**
  - **Benefits**
  - **IP delivery**
  - **ESD testing and consulting**

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Sofics on-chip ESD clamps protect a broad range of applications and technologies

3000+ products

rely on Sofics ESD protection

50+ different processes

including CMOS down to 28nm, BCD, SOI...

50+ fabless customers

include Sofics ESD IP for beyond standard IOs

70+ customers

protect chip interfaces with Sofics ESD

75+ patents

in Sofics' clean ESD IP portfolio

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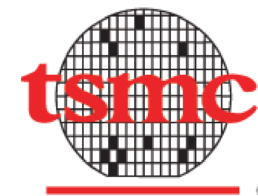
Sofics Customers

Specialty ESD clamps available



Open Innovation Platform®

- Broad solution coverage on TSMC technology
  - Portable to other nodes/domains/foundries

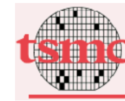
Node	Voltage domains
350nm HV	3.3V, 15V
250nm BCD, gen. I and II	12V, 24V, 40V, 60V >>> PowerQubic license TSMC-Sofics
180nm BCD, gen. I and II	18V, 24V, 32V, 40V, 60V
180nm CMOS	1.8V, 3.3V, 5V
130nm CMOS	1.0V, 1.2V, 3.3V, 5V, 7V
90nm CMOS	1.2V, 1.8V, 3.3V
65nm CMOS	1.0V, 1.2V, 1.8V, 2.5V, 3.3V, 5V
40nm CMOS	0.9V, 1.2V, 1.8V, 3.3V, 5V
28nm CMOS	0.85V, 0.9V, 1.8V, 3.3V, 5V, 5.5V, 12V
16nm FinFET	Preparing a first tape out (H2 2015)

Sofics fabless customers

- Sofics customers working on foundry platforms
  - Use standard IO libraries from the foundry / IO providers
    - Includes free delivery of ESD
    - Covers maybe 90% of their interface requirements
  - Use foundry ESD guidelines to build own IO+ESD libraries
    - E.g. Custom output driver circuits
  - Use Sofics ESD solutions for special, custom designed interfaces
    - High speed interfaces that require low capacitive ESD clamps
    - Wireless interfaces
    - Overvoltage tolerant IO's
    - Low leakage analog interfaces
    - Protection of interfaces for very high ESD requirements (8kV HBM or more)
    - Or a combination of above

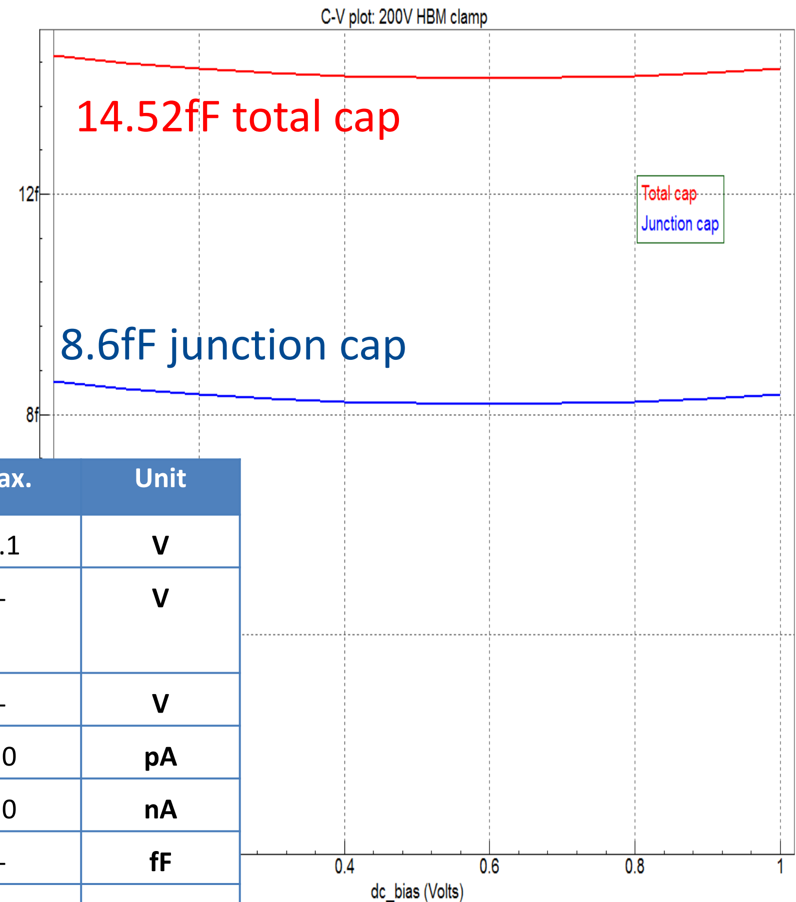
TakeCharge: ESD solutions for up to 5V CMOS

- >50 customers, broad application space, various foundries
  - High speed digital interfaces
    - USB, HDMI up to 6Gbps, SerDes up to 28Gbps
    - Wireline communication, optical communication, several Gbps
  - Wireless applications (GPS, NFC, bluetooth...) up to 10 GHz
  - FPGA IO protection in 180nm to 28nm CMOS
  - Smartcard, security, M2M applications
  - Generic ASIC protection libraries
  - Power Management ICs
  - Computing applications
    - Ultra low power MCUs
    - Image processors
  - CMOS Imager sensors
  - Medical applications
  - ...



Case 1 - Optical communication

- TSMC 28nm Sofics solution
  - <15 fF total parasitic capacitance
  - 200V HBM
  - Protection of LV I/O



Excerpt from datasheet

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage	- 0.3	1	1.1	**V**
Trigger Voltage	-	VSS-0.3V VDD+0.3V	-	**V**
Holding Voltage	-	1.24	-	**V**
IO Leakage current @ T_{amb} = 25 °C, 1V DC	-	10	50	**pA**
IO Leakage current @ T_{amb} = 125 °C, 1V DC	-	10	50	**nA**
Capacitance Load of Junctions (@0V bias)	-	8.6	-	**fF**
Total capacitance at I/O (@0V bias)	-	14.52	-	**fF**
HBM – Human Body Model	-0.2	-	+0.2	kV

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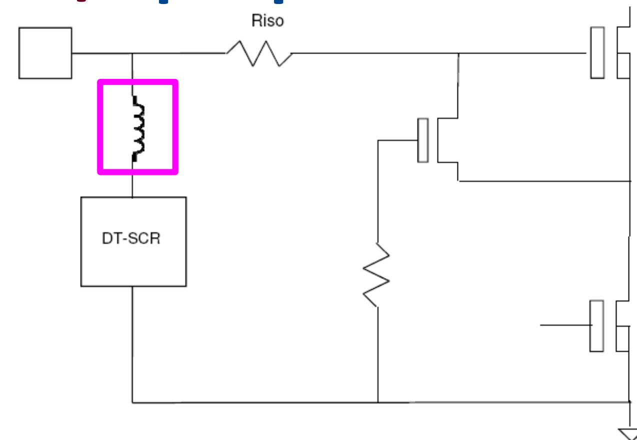
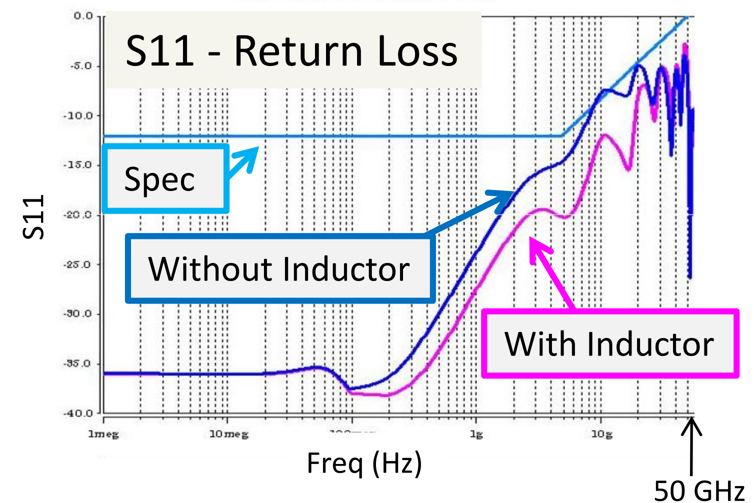
SOFICS Solutions For ICs

Case 2 - TSMC 28nm: 28Gbit/s pin protection



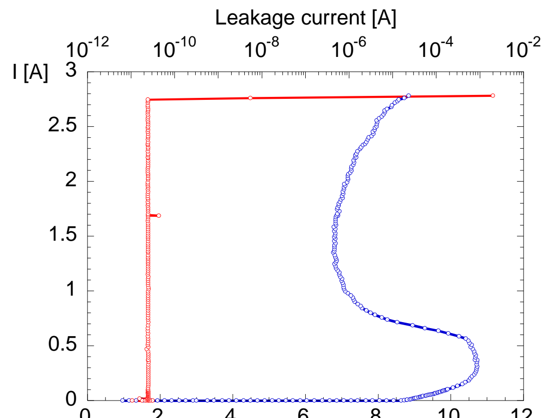
- Normal operation specifications
  - Low cap
    - DTSCR + reverse diode + metal: 80fF
  - Low Return loss
    - Inductor in series with SCR lowers S11 peaks at ~10GHz and 20GHz
- ESD specifications
  - > 1kV HBM
    - Higher not measured
  - 300V CDM
    - 4.5A CDM peak current

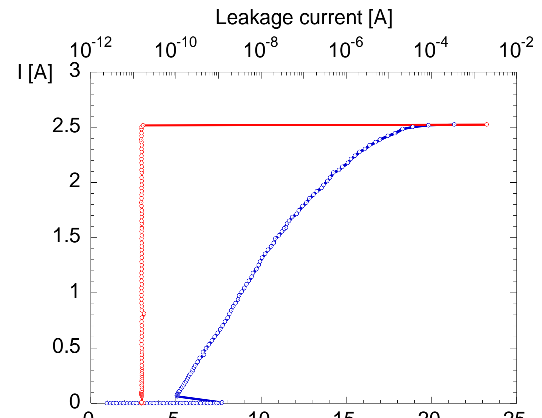


Case 3 - HV interfaces in 28nm

- Customer required different high voltage ranges in TSMC 28nm

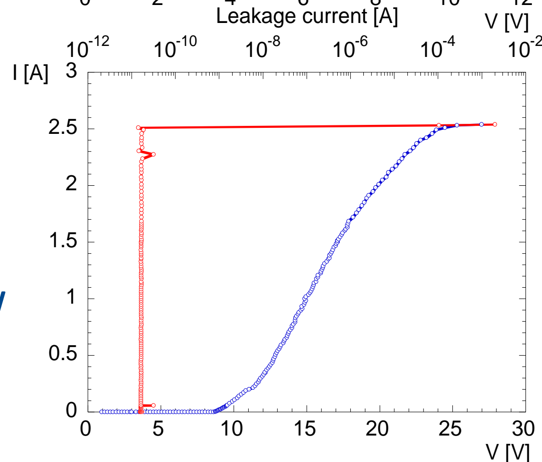
3.9V
5.5V
6.05V
no DNW

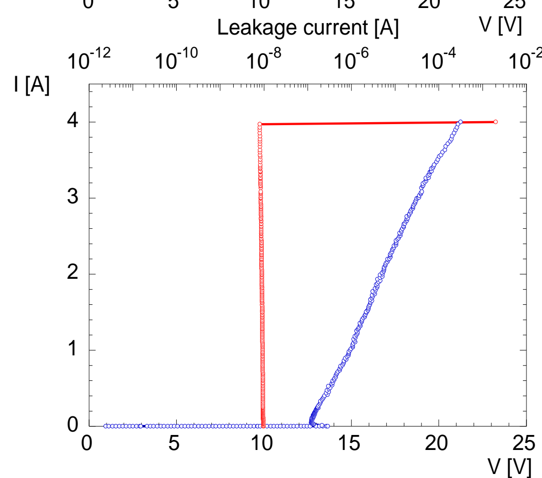




3.9V
with DNW

5.5V
6.05V
with DNW



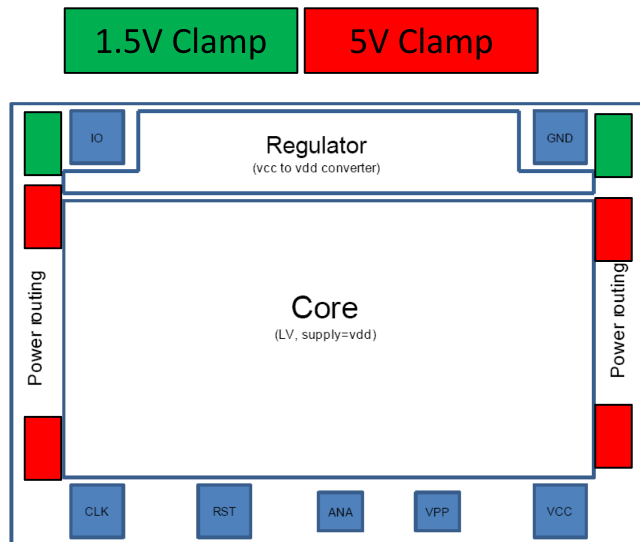


13.2V
with DNW

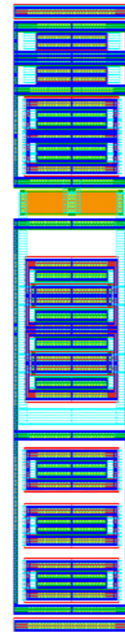
Case 4 - protection in new process

- Product processed in Grace Semiconductor 0.13um Technology
  - Technology was at time untested by Sofics
- First time right required

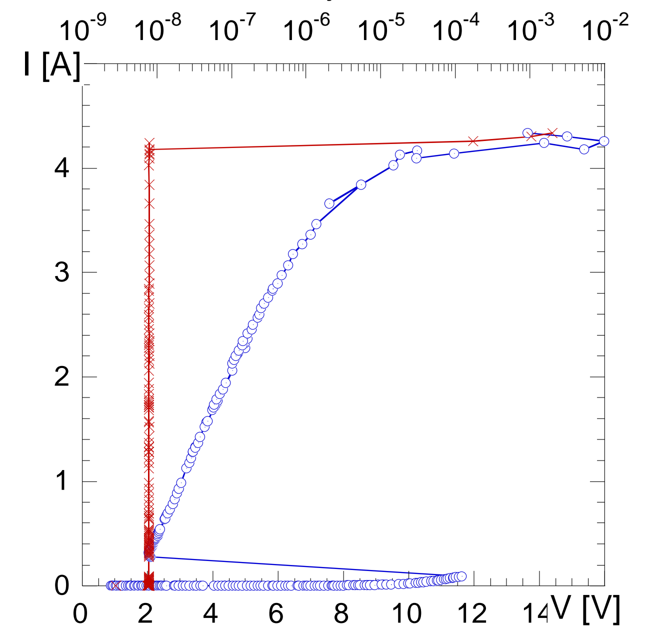
Placement



Layout



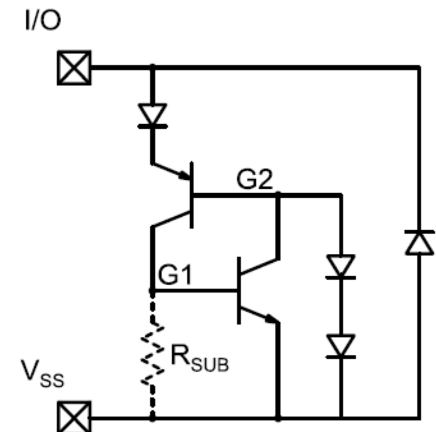
Analysis



Case 5 - High ESD protection levels

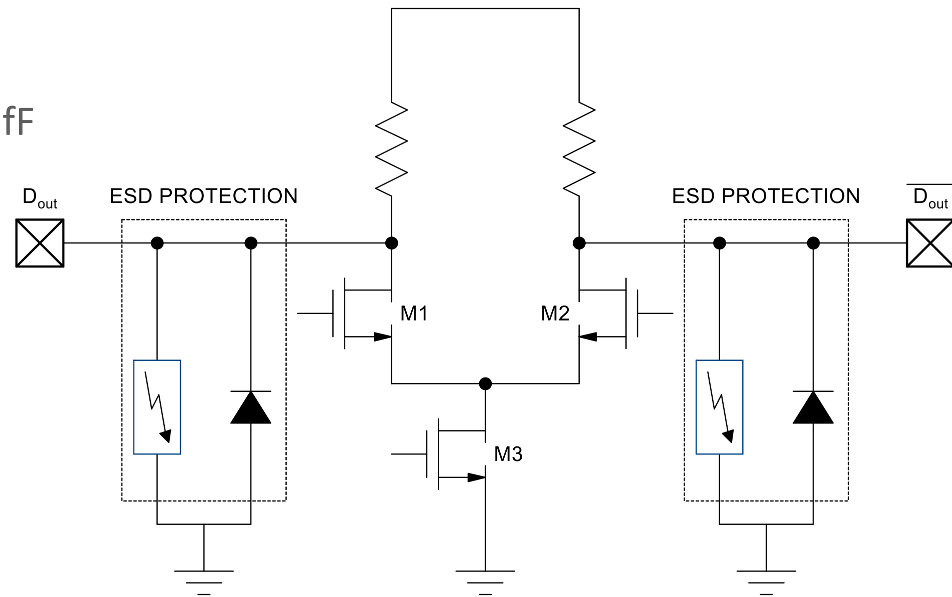
- High definition Serial interface protection
  - TSMC 40nm LP
  - 3Gbps interfaces – Video signals
  - Total parasitic capacitance at IO <300fF
  - High ESD protection required >4kV HBM
- Sofics delivery
  - Custom ESD clamp
    - Optimized for low junction and metal capacitance
      - Parasitic junction capacitance: 150fF
      - Parasitic metal capacitance: 50fF
      - Bondpad capacitance: 100fF
  - Area: $1300 um^2$
  - Achieved 5kV HBM

Circuit schematic



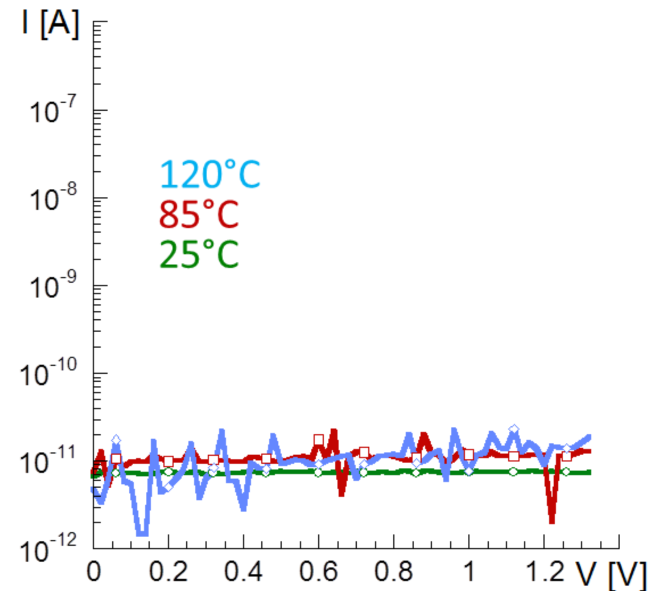
Case 6 - HDMI with 50 Ohm termination

- High speed, high ESD protection (0.13um)
  - 50 Ohm Termination: No diode to Vdd
  - > 8kV HBM requested
  - Local Sofics clamp placed
    - Leakage < 10nA
    - Junction capacitance: 587 fF
    - Area 2,830 um2
    - ESD performance
      - TLP > 6.5A
      - HBM > 8kV



Case 7 - Protect ultra low leakage interfaces

- Reduce ESD related leakage with Sofics ESD IP
  - Example: 1.2V TSMC 40nm
    - ESD protection for RF LNA circuit
    - Leakage ~20pA at 1.2V at high temperature
  - Example: 5V TSMC 180nm
    - ESD protection for overvoltage tolerant IO
    - Leakage ~10nA at 5V at high temperature
  - Example: 65nm ESD cells
    - All kinds of voltage domains
    - All kinds of interface types
    - Leakage ~20nA at high temperature



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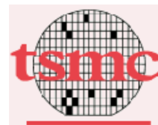
PowerQubic ESD solutions for High Voltage interfaces

- >20 product implementations
  - Several customers
  - >20 projects
  - Different product types supported
    - Automotive LIN Transceivers
    - Automotive sensors (Temp, humidity, Air flow)
    - Automotive LED drivers
    - Industrial CAN interface
    - Industrial DAC
    - Industrial High Voltage RS485
    - Li-ion battery control
    - Switching/power regulator
    - Hearing implant interface protection



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Products – Test service

- Fully equipped ESD test lab
  - **HBM & MM** ANSI/ESDA and JEDEC on packaged dies
  - **CDM** through partnership
  - **Latch-up** JEDEC on packaged dies
  - **TLP** on packaged and bare dies
    - Pulse width options: 75ns and 100ns
    - Rise time options: 200ps, 2ns, 10ns, 20ns
  - **VF-TLP** on bare dies
    - Pulse width options: 1ns, 2ns, 5ns and 10ns
    - Rise time options: 100ps, 200ps, 2ns
  - **DC** leakage and IV tracing on packaged and bare dies
  - **Solid state pulsing** on packaged and bare dies
  - **Thermo chuck** for measurements up to 200°C
  - **Teseq NSG 438** ESD zap gun for IEC 61000-4-2 tests

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