Sofics is a foundry-independent IP provider

• **Semiconductor IP provider**
  – Sofics = “Solutions for ICs”
  – IP portfolio
    ▪ Since 2000: On-chip ESD protection for CMOS, SOI applications up to 5V
    ▪ Since 2010: On-chip ESD protection for applications 5V to 100V
  – New (non-ESD) portfolio’s under development

• **Consulting**
  – On-chip ESD protection support

• **Test lab**
  – ESD relevant analysis
  – Transmission Line Pulsers, HBM, MM, Latch-up, IEC 61000-4-2
Sofics on-chip ESD clamps protect a broad range of applications and technologies.

1 IC release per day
includes Sofics on-chip ESD protection

50+ different processes
including CMOS down to 28nm, BCD, SOI...

50+ fabless customers
include Sofics ESD IP for beyond standard IOs

70+ customers
protect chip interfaces with Sofics ESD

75+ patents
in Sofics’ clean ESD IP portfolio
SOFICS supports 70+ IC companies worldwide
3 main reasons why IC designers rely on Sofics solutions

Reduce IC cost
lower development, design, silicon and manufacturing costs

Pass any ESD/EOS/LU specification
flexible technology adapts to your requirements

Enhance IC performance
lowest leakage, capacitance ...
Specialty ESD clamps available

- Broad solution coverage on TSMC technology
  - Portable to other nodes/domains/foundries

<table>
<thead>
<tr>
<th>Node</th>
<th>Voltage domains</th>
</tr>
</thead>
<tbody>
<tr>
<td>350nm HV</td>
<td>3.3V, 15V</td>
</tr>
<tr>
<td>250nm BCD, gen. I and II</td>
<td>12V, 24V, 40V, 60V &gt;&gt;&gt; PowerQubic license TSMC-Sofics</td>
</tr>
<tr>
<td>180nm BCD, gen. I and II</td>
<td>18V, 24V, 32V, 40V, 60V</td>
</tr>
<tr>
<td>180nm CMOS</td>
<td>1.8V, 3.3V, 5V</td>
</tr>
<tr>
<td>130nm CMOS</td>
<td>1.0V, 1.2V, 3.3V, 5V, 7V</td>
</tr>
<tr>
<td>90nm CMOS</td>
<td>1.2V, 1.8V, 3.3V</td>
</tr>
<tr>
<td>65nm CMOS</td>
<td>1.0V, 1.2V, 1.8V, 2.5V, 3.3V, 5V</td>
</tr>
<tr>
<td>40nm CMOS</td>
<td>0.9V, 1.2V, 1.8V, 3.3V, 5V</td>
</tr>
<tr>
<td>28nm CMOS</td>
<td>0.85V, 0.9V, 1.8V, 3.3V, 5V, 5.5V, 12V</td>
</tr>
<tr>
<td>16nm FinFET</td>
<td>Taped out ESD test chip (July 2015)</td>
</tr>
</tbody>
</table>
TakeCharge: ESD solutions for up to 5V CMOS

• >50 customers, broad application space, various foundries
  – High speed digital interfaces
    ▪ USB, HDMI up to 6Gbps, SerDes up to 28Gbps
    ▪ Wireline communication, optical communication, several Gbps
  – Wireless applications (GPS, NFC, bluetooth...) up to 10 GHz
  – FPGA IO protection in 180nm to 28nm CMOS
  – Smartcard, security, M2M applications
  – Generic ASIC protection libraries
  – Power Management ICs
  – Computing applications
    ▪ Ultra low power MCUs
    ▪ Image processors
  – CMOS Imager sensors
  – Medical applications
  – ...

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Case 1 - Optical communication

- TSMC 28nm Sofics solution
  - <15 fF total parasitic capacitance
  - 200V HBM
  - Protection of LV I/O

Excerpt from datasheet

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>-0.3</td>
<td>1</td>
<td>1.1</td>
<td>V</td>
</tr>
<tr>
<td>Trigger Voltage</td>
<td>-</td>
<td>VSS-0.3V</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDD+0.3V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Holding Voltage</td>
<td>-</td>
<td>1.24</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>IO Leakage current @ $T_{amb} = 25 , ^\circ$C, 1V DC</td>
<td>-</td>
<td>10</td>
<td>50</td>
<td>pA</td>
</tr>
<tr>
<td>IO Leakage current @ $T_{amb} = 125 , ^\circ$C, 1V DC</td>
<td>-</td>
<td>10</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>Capacitance Load of Junctions (@0V bias)</td>
<td>-</td>
<td>8.6</td>
<td>-</td>
<td>fF</td>
</tr>
<tr>
<td>Total capacitance at I/O (@0V bias)</td>
<td>-</td>
<td>14.52</td>
<td>-</td>
<td>fF</td>
</tr>
<tr>
<td>HBM – Human Body Model</td>
<td>-0.2</td>
<td>-</td>
<td>+0.2</td>
<td>kV</td>
</tr>
</tbody>
</table>
Case 2 - TSMC 28nm: 28Gbit/s pin protection

- Normal operation specifications
  - Low cap
    - DTSCR + reverse diode + metal: 80fF
  - Low Return loss
    - Inductor in series with SCR lowers S11 peaks at ~10GHz and 20GHz

- ESD specifications
  - > 1kV HBM
    - Higher not measured
  - 300V CDM
    - 4.5A CDM peak current
Case 3 - HV interfaces in 28nm

- Customer required different high voltage ranges in TSMC 28nm

3.9V  
5.5V  
6.05V  
no DNW

5.5V  
6.05V  
with DNW

13.2V  
with DNW

3.9V  
with DNW
Case 4 - protection in new process

- Product processed in Grace Semiconductor 0.13um Technology
  - Technology was at time untested by Sofics
- First time right achieved
  - 1.5V, 5V, 10V clamps
Case 5 - High ESD protection levels

• High definition Serial interface protection
  – TSMC 40nm LP
  – 3Gbps interfaces – Video signals
  – Total parasitic capacitance at IO <300fF
  – High ESD protection required >4kV HBM

• Sofics delivery
  – Custom ESD clamp
    ▪ Optimized for low junction and metal capacitance
      – Parasitic junction capacitance: 150fF
      – Parasitic metal capacitance: 50fF
      – Bondpad capacitance: 100fF
  – Area: 1300um²
  – Achieved 5kV HBM
Case 6 - HDMI with 50 Ohm termination

- High speed, high ESD protection (0.13um)
  - 50 Ohm Termination: No diode to Vdd
  - > 8kV HBM requested
  - Local Sofics clamp placed
    - Leakage < 10nA
    - Junction capacitance: 587 fF
    - Area 2,830 um2
    - ESD performance
      - TLP > 6.5A
      - HBM > 8kV
Case 7 - Protect ultra low leakage interfaces

• Reduce ESD related leakage with Sofics ESD IP
  – Example: 1.2V TSMC 40nm
    ▪ ESD protection for RF LNA circuit
    ▪ Leakage ~20pA at 1.2V at high temperature
  – Example: 5V TSMC 180nm
    ▪ ESD protection for overvoltage tolerant IO
    ▪ Leakage ~10nA at 5V at high temperature
  – Example: 65nm ESD cells
    ▪ All kinds of voltage domains
    ▪ All kinds of interface types
    ▪ Leakage ~20nA at high temperature
PowerQubic ESD solutions for High Voltage interfaces

- >20 product implementations
  - Several customers
  - >20 projects
  - Different product types supported
    - Automotive LIN Transceivers
    - Automotive sensors (Temp, humidity, Air flow)
    - Automotive LED drivers
    - Industrial CAN interface
    - Industrial DAC
    - Industrial High Voltage RS485
    - Li-ion battery control
    - Switching/power regulator
    - Hearing implant interface protection
Products – Test service

• Fully equipped ESD test lab
  – HBM & MM ANSI/ESDA and JEDEC on packaged dies
  – CDM through partnership
  – Latch-up JEDEC on packaged dies
  – TLP on packaged and bare dies
    ▪ Pulse width options: 75ns and 100ns
    ▪ Rise time options: 200ps, 2ns, 10ns, 20ns
  – VF-TLP on bare dies
    ▪ Pulse width options: 1ns, 2ns, 5ns and 10ns
    ▪ Rise time options: 100ps, 200ps, 2ns
  – DC leakage and IV tracing on packaged and bare dies
  – Solid state pulsing on packaged and bare dies
  – Thermo chuck for measurements up to 200°C
  – Teseq NSG 438 ESD zap gun for IEC 61000-4-2 tests
Contact us

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