A geometry scalable approach to InP HBT compact modeling for mm-wave applications

T. Nardmann[1], P. Sakalas[1], Frank Chen[3], T. Rosenbaum[1], M. Schroter[1,2]

[1]Chair for Electron Devices and Integrated Circuits, Technical University Dresden, 01062 Germany
[2]ECE Dept., UC San Diego, La Jolla, CA 92093, USA
[3]GCS Corporation, Torrance, CA 90505, USA

***Abstract* - The bias and frequency dependent scaling of InP/ InGaAs HBTs with emitter *width* (and length) has been investigated for a 300GHz foundry process. It was found that the currents, capacitances and resistances related to the emitter dimensions scale quite well. This allows the use of special test structures in combination with geometry variations to distinguish different physical effects and to accurately determine the external elements of the transistor as well as the thermal resistance independently of each other. The approach enables the generation of a geometry scalable set of HICUM/L2 model parameters for a large geometry range. The model was compared to experimental DC, AC and large-signal data of devices with different emitter geometry. The good agreement offers a much wider range of options for optimizing high-speed InP circuits.**

Index Terms - Heterojunction bipolar transistors, Indium-Phosphide, Compact modeling, HICUM/L2.

I Introduction

InP HBTs are a promising contender for mm-wave circuits and systems and their extension into the THz realm [1, 2]. One of the obstacles of deploying InP technology in production circuit design is the lack of accurate transistor models (e.g. [3]). The demand for the latter has been documented by various attempts for improved compact models (e.g. [4, 5]). Since these attempts (incl. the use of VBIC) are based on the SPICE Gummel-Poon model (SGPM), which is not even adequate anymore for describing modern BJTs, the extensions tend to remain patchy and lack a solid physical basis. As a consequence, the effort for extracting the (too) many fitting parameters allows to provide model parameter sets for very few (typ. 3 to 5) different device sizes only. Also, the model accuracy suffers since a reliable extraction of parameters such as the base and collector resistance as well as the proper partitioning of capacitances is not possible based on data from just a single device geometry [6]. These problems severely limit circuit optimization and, thus, the exploitation of the true potential of InP HBT technology.

Variation of especially the emitter width b_{E0} allows to separate many physical effects and to determine series resistances and capacitances of different device regions accurately, thus not only resulting in the model to accurately represent important time constants but also enabling statistical design. The latter is especially important for InP process technologies due to their relatively low volume and somewhat larger process variability (compared to e.g. SiGe BiCMOS technology).

The issues described above (and several others) can be overcome with a physics-based geometry scalable modeling approach that has been used successfully for HICUM/L2 [7] by all major SiGe BiCMOS foundries for many years (e.g. [8, 9]. Rather than being limited to a single simulator (like special III-V HBT models), HICUM/L2 has been an industry-wide standard model since 2004 and has been available in a uniform and numerically stable implementation in all mainstream commercial circuit simulators. Most recently, HICUM/L2 has been applied to InGaAs/InP HBTs fabricated in various process technologies. First results using the simplified HICUM/L0 [7] were encouraging [10]. However, the lack of suitable test structures and, thus, the necessity of having to *fit* data of just a single device still did not allow an accurate determination of many elements of the equivalent circuit. In this paper, a geometry scalable modeling approach is presented, which enabled the switch to HICUM/L2. The corresponding experimental results are based on a special test chip designed and fabricated in a foundry process [11]. As a consequence of this work, similar circuit design capability as for Si-based technologies [12, 8, 9] can now be offered also for InP HBTs, hopefully aiding a more rapid deployment of this technology in prototypes and products.

II Geometry Scalable Parameter extraction

In the equivalent circuit of HICUM/L2 each element represents a particular device region. The physical effects in that device region are captured by the analytical bias, temperature and geometry dependent description of the elements [7]. Since some geometry related effects can only be accurately described by quite sophisticated equations such as Green's functions the geometry dependence is typically not included in the model card or even the Verilog-A model code. The "absolute" HICUM/L2 model parameters are thus usually generated from *technology specific* parameters, such as sheet resistances as well as saturation currents and capacitances per area and perimeter length, and the given design rules of a process [7]. While this approach guarantees physics-based values for the equivalent circuit elements, it does require a somewhat larger initial effort regarding test structure layouts and parameter extraction.

In this work, a set of special test structures was designed and fabricated which allowed to determine the required *technology specific* parameters of all transistor regions separately. In addition, with clever layouts, e.g., the collector and base resistance can also be measured directly on some of the structures. The examples shown below illustrate the approach.

The internal and external base resistance components R_{Bi} and R_{Bx} can be measured and also clearly separated using a tetrode

structure [13]. For III-V HBTs, the latter typically reduces to a more simple "walled emitter" structure as shown in Fig. 1(a). The corresponding cross section indicates the two components that can be directly determined from this structure. Their values are the same as for a transistor with the same dimensions (b_{E0}<<length l_{E0}). By varying just the emitter width, the sheet resistance R_{SBi} of the internal base layer can be measured (cf. Fig. 1(b)) as a function of bias (cf. Fig. 1(c)). The latter result allows to determine the zero-bias hole charge Q_{p0} of the model. The R_{Bi} value for other transistor geometries is then simply calculated from R_{SBi} and the emitter dimensions as well as the configuration (number of stripes, contact arrangement) as described in [14]. A simple contact chain for the external base region allows to determine the base contact resistance and the external base sheet resistance (here the same as the zero-bias value R_{SBi0}). Again, using these specific parameters, the external base resistance can be accurately calculated for any dimensions and contact configuration [14]. A similar approach is applied to the external collector resistance.

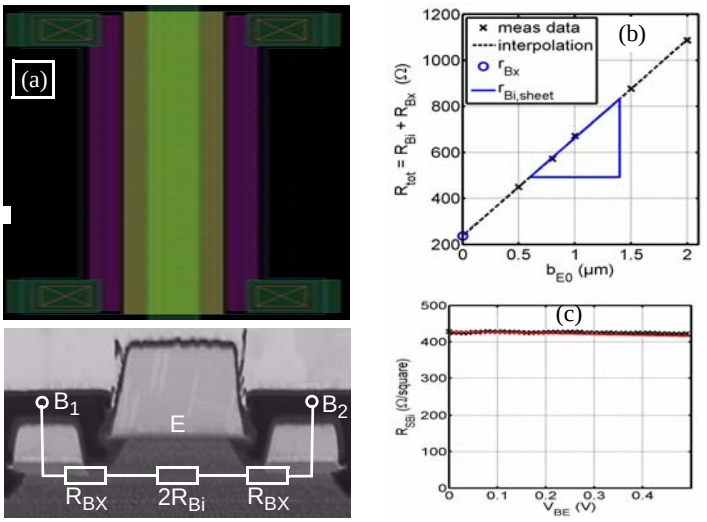

Fig. 1: Tetrode structure used for determining the base resistance components: (a) Layout and schematic cross-section with components. (b) Measured total resistance vs. b_{E0} with extracted sheet resistance R_{SBi} and external base resistance R_{Bx} for a given length l_{E0} = 15µm. (c) Bias dependent R_{SBi} measurement (symbols) and model (solid line).

The emitter width dependence of the collector transfer current is shown in Fig. 2(a) for groups of transistors with different emitter length l_{E0}. According to these results, the process exhibits excellent scalability and there is no reason why this feature should not be employed for circuit optimization. The total current is then simply given by

$$I_T = J_{TA}A_E + J_{TP}P_E + J_{T0}\,, \qquad (1)$$

from which the corresponding area and perimeter related current component, J_{TA} and J_{TP}, can be easily determined using long structures. Note that the typically employed approach (e.g. [15]) shown in Fig. 2(b) does not work here due to the negative slope. This can be resolved though by introducing effective electrical emitter dimensions b_E and l_E, which describe the dimensions of the actual injecting jucntion ao as to reduce J_{T0} to zero. Eq. (1) has also been applied to the base current as well as to the depletion capacitances.

Due to the severe self-heating, complete sets of characteristics including those of the special test structures were measured for different temperatures T (= 300, 325, 350, 375K) in order to extract the various temperature coefficients and the thermal resistance R_{th} along with thermal coupling coefficients between multiple emitter fingers. The latter were determined from a special test structure with sense and force contacts. Fig. 3(a) shows the resulting emitter area dependence of R_{th}, which can be well approximated by

$$R_{th} = R_{th0}/(1 + a_{thb}b_{E0} + a_{thl}l_{E0})\,, \qquad (2)$$

where R_{th0} and the a_{th} factors are parameters.

The emitter resistance R_E was extracted according to [16]. Its geometry dependence is shown in Fig. 3(b).

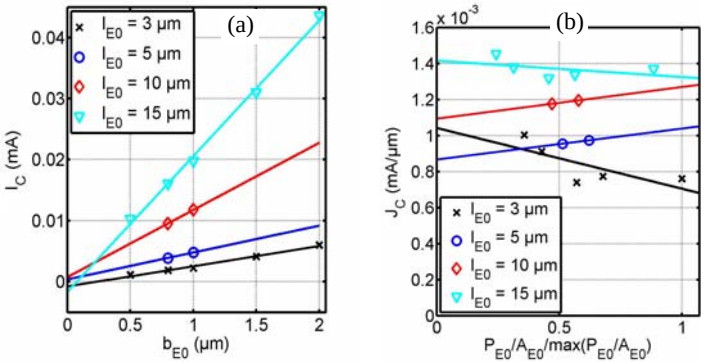

Fig. 2: Measured transfer current at (V_{BE}, V_{BC}) = (0.6, 0)V for devices with different emitter dimensions. Data of all devices as function of (a) emitter width b_{E0} and (b) perimeter length to area ratio P_{E0}/A_{E0}.

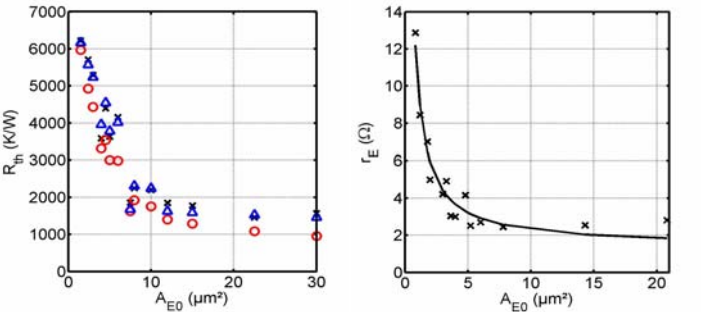

Fig. 3: Emitter dimension dependence: (a) thermal resistance from measurements (crosses), eq. (2) (triangles), and 3D thermal simulation (circles). (b) Emitter resistance from measurements (crosses) and model (line).

For determining the remaining model parameters, the characteristics of all devices were measured up to the highest possible current densities and collector-emitter voltages, which were limited by the severe self-heating. For instance, the transit frequency f_T could be measured for higher voltages only up to about its peak current density. As a consequence, the extraction of model parameters for the high-current region, which also determine the shape of the peak region, was more difficult due to the lack of sufficient data in that region. Here, pulsed bias dependent S-parameter measurements are certainly preferable for significantly extending the range of the data. Such a set-up is presently being built and is planned to be used for obtaining

more suitable data for the final version of this paper.

III Model comparison with Experimental Results

A large number of transistors with different emitter dimensions and configurations were fabricated. Their characteristics were compared over bias and temperature with HICUM/L2. Only the long devices mentioned earlier were used for parameter extraction. Based on the technology specific parameters and design rules, the absolute model parameters of all devices were then generated by a special scaling tool [17]. Due to the lack of space, only selected comparisons can be shown below, which are subdivided into the geometry dependence and bias dependence. All results are presented for T = 300K but with self-heating included. The standard pad size available for the process allowed only external (i.e. ISS) calibration (vs. on-chip calibration) and thus S-parameter measurements up to 50GHz.

A. Geometry dependence

A comparison of bias dependent characteristics of devices with different emitter geometry is shown in Fig. 4. The collector saturation current scaling according to eq. (1) guarantees an accurate representation of I_C at low injection for different emitter widths and areas (cf. Fig. 4(a)). At higher injection levels the proper scaling of mostly the series resistances and thermal resistance become relevant. Due to the superposition of various effects, an accurate determination of these resistances and their temperature dependence from dedicated separate test structures is mandatory.

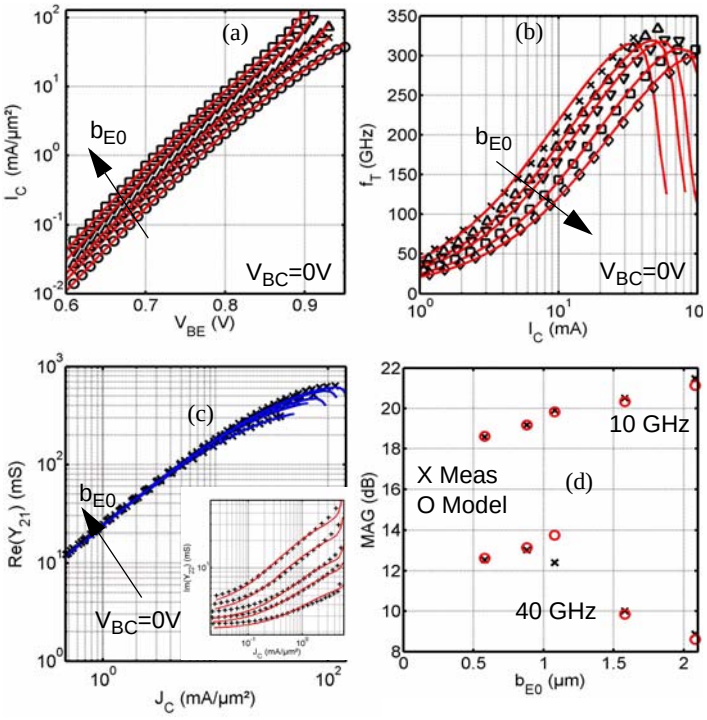

Fig. 4: Comparison between measurement (symbols) and HICUM/L2 (lines) for HBT with different *emitter widths* b_{E0} = (0.5, 0.8, 1, 1.5, 2) µm. (a) Collector current I_C vs. V_{BE}. (b) Transit frequency f_T vs. I_C. (c) Real(y_{21}) and, in the inset, Imag(y_{22}) vs. I_C at 10 GHz. (d) maximum available/stable gain vs. emitter width for f = (10, 40) GHz and at J_C = 1mA/µm^2.

The peak of the transit frequency f_T in Fig. 4(b) exhibits only a weak dependence on emitter width. Its geometry scaling is determined by the separate scaling of the BE and BC depletion capacitances, the emitter and collector resistance and the transconductance as well as the transit time. The real part of y_{21} at 10GHz, which basically corresponds to the transconductance, is indeed described quite well in Fig. 4(c) from low to high injection over the investigated emitter width range. The inset shows imag(y_{22}), which corresponds to the BC capacitance at low current densities, but then exhibits quite a strong current dependence at higher injection. Finally, Fig. 4(d) shows the emitter width dependence of the maximum available gain for both 10GHz and 40GHz at J_C = 1mA/µm^2, which is a typical operating point. While for 10GHz MAG increases by about a factor 4 (from 0.5 to 2µm), it decreases by about the same factor for 40GHz. This may be attributed to significant dynamic emitter current crowding (i.e. a decrease in the emitter utilization factor) in the wide devices.

B. Bias dependence

To assess specifically the suitability and accuracy of HICUM/L2 for InP HBTs, a large variety of bias, frequency and temperature dependent characteristics were compared for various emitter geometries. Due to the lack of space only selected bias dependent results are shown for A_{E0}=0.8*15µm^2 at T_{chuck}=300K.

The transfer characteristics were already shown to be accurately described in Fig. 4(a). A clear indication of the temperature dependent modeling and the impact of self-heating is obtained by considering the output characteristics for constant V_{BE}. The excellent agreement observed in Fig. 5(a) between model with self-heating and the measurement also confirms the accuracy of the base current description. For reference, the model results without self-heating have also been added. The comparison of the bias dependent transit frequency in Fig. 5(b) confirms the suitability of the model (from Si based applications) for accurately describing the charges in an InP HBT especially also in the high-current region and in saturation (i.e. low V_{CE}). It is interesting to note that the measured data behave very similar to SiGe HBTs. Only at high V_{CB} the curves start crossing each other, which is partly caused by the self-heating though and still captured by the model.

The maximum available power gain in Fig. 5(c) is also quite well described over a wide collector current density and frequency range. Finally, the large-signal behavior of the model was investigated using the load-pull measurements shown in Fig. 5(d). The fundamental frequency was set to 15GHz and a two-tone signal with 10MHz spacing was applied to the input (base) terminal. Sweeping the input power to sufficient high levels causes significant distortion in the collector current due to the transistor nonlinearity. Fig. 5(d) shows the total signal levels of the third and fifth harmonics that result from backmixing into the fundamental band. The model produces the same trend as the measurements, although the kink in the fifth harmonics occurs at somewhat too low Pin. Note that comparing the distortion related signals in the same band as the fundamental frequency allows to push the model verification frequencies towards the limits of the spectrum analyzer typically available in a characterization lab without having to resort to downconverters and the associated

added uncertainty in on-wafer transistor measurements.

The causes for the remaining deviations are presently under investigation. Once more data have been evaluated and the causes have been identified, the deviations are expected to be further reduced.

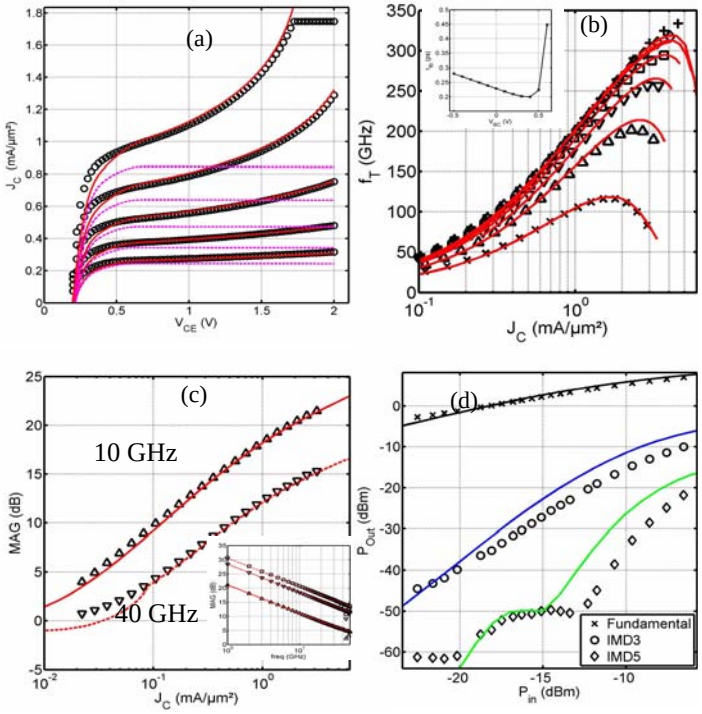

Fig. 5: Comparison between measurement (symbols) and HICUM/L2 (lines) for an HBT with A_{E0} = 0.8*15 µm². (a) Output characteristics for V_{BE} = (0.8, 0.815, 0.83, 0.845, 0.86)V, showing the impact and correct modeling of self-heating (the dashed lines correspond to the isothermal model without self-heating). (b) Transit frequency f_T for V_{BC} = -(0.25, 0, 0.1, 0.2, 0.3, 0.4, 0.5)V. (c) Maximum available gain vs. collector current density at V_{BC} = -0.25V and (10, 40) GHz. (d) Output power vs. input power for the fundamental frequency f_1 = 15 GHz and in-band intermodulation distortion at J_C = 1mA/µm² and V_{CE} = 1V.

IV Summary and Conclusions

Scaling of InP/InGaAs HBTs with emitter *width* and length has been investigated for a 300GHz foundry process. It was found that all current, capacitances and resistances related to the emitter dimensions scale quite well. This allows to use special test structures in combination with geometry variations to distinguish different physical effects and to accurately determine the technology specific parameters of the process independently of each other. Applying a geometry scaling tool then enables to generate sets of HICUM/L2 model parameters for a wide range of emitter dimensions and configurations. The good agreement of the model with experimental DC, AC and large-signal data enables not only the optimizing high-speed InP circuits but also the generation of statistical models and, thus, the incorporation of the impact of process tolerances during circuit design. This paper shows that there is no reason why these features should not be available for InP HBT technology.

Since HICUM/L2 is widely available in commercial circuit simulators and production tested for SiGe BiCMOS technologies, the deployment of process design kits is not bound to specific circuit simulators. Compared to the standard version of HICUM/L2 just a few small changes were required to described the InP HBTs presented in this paper. None of the bias dependent equations of the core model formulation had to be changed.

V Acknowledgments

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