I/O interface design : An overview

A Chip communicates to the external world through its interface cells called Input/output (I/O) buffers. The primary function of an I/O buffer is to either receive the signals into the core of the chip or transmit them to the external world. Since I/O buffers are in direct contact with the external world, they are equipped with protective devices (Electro-Static Discharge clamps) to protect the chip from high voltage surges. With the evolution of Mobile communications and networking, there is a growing demand for high-speed and high-performance chips. This requires Input/Output (I/O) buffers to be more versatile and complex. The design of I/O buffers incorporates programmability in drive strength, slew rates, output impedance, output voltage swing etc. Complexity of the buffers also increases as the chips need buffer characteristics to be independent of Process, Voltage and Temperature (PVT) variations. Proper functioning of an I/O buffer is important to the operation and reliability of the chip.

Top-down placement and packaging methodology of an IC is shown in Fig-1. All I/O cells are usually placed in the periphery of the chip with memory, analog and core cells placed inside. A typical IO interface design takes care of various wire-bonding or flip-chip packaging options.

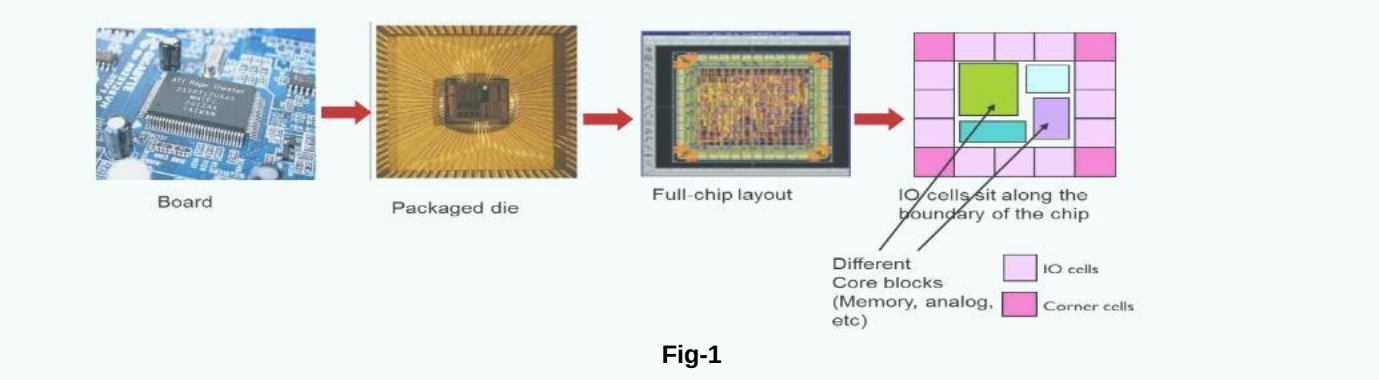


Fig-1

Since an I/O buffer interacts with the external world, it can be subjected to static charges. This can be well understood from Fig-2. As shown in Fig-2, if a charged human body touches a pin of an IC, static charges stored on the human body will find a least resistive path to discharge. If any other pin of the same IC is at a different potential from the pin that is touched by the human body, it leads to flow of high current for a short duration. This flow of high current may potentially damage the pin (and other internal circuitry connected to that pin) if sufficient protection is not built along with the buffer that is connected to the pin. This protection is referred to as Electro-static discharge (ESD) protection.

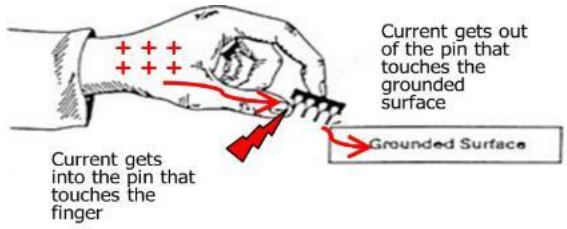


Fig-2

Importance of I/O buffers:

- Interface between core of chip and external world
- To drive huge and different types of loads
- Drive/receive both low-frequency and high-frequency signals without significant attenuation
- Immunity from external noise for the signal
- Electro-static discharge protection

Depending on the various requirements for data transfer, I/O buffer could be designed as single-ended or fully differential as shown in Fig-3.

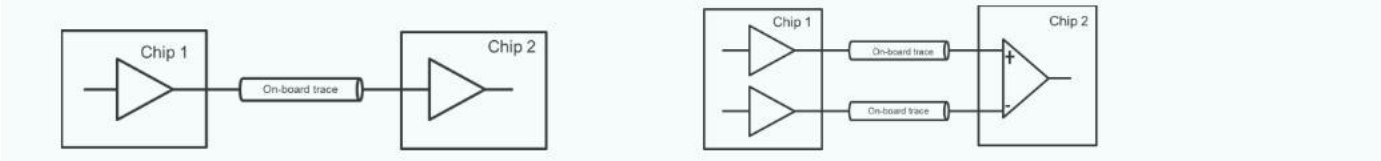
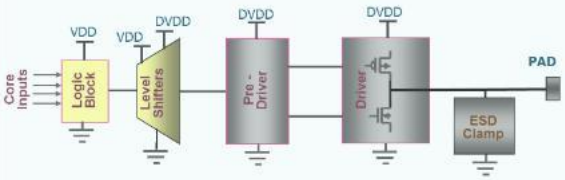


Fig-3

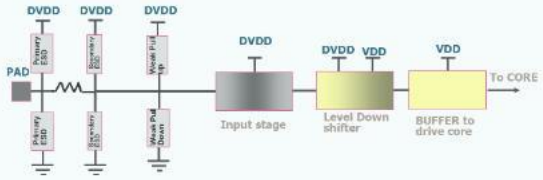
Basic building blocks of an output buffer and input buffer are presented in Fig-4. Design of each block gets complicated as the specification requirements get complex. There are applications where the same external pin can act as an output buffer as well as input buffer.

Output buffer



- **Logic Block :** processes the core signals and decides the state/function of I/O
- **Level shifters :** shift the core signals' level to I/O supply level.
- **Pre-driver :** liaison between level-shifters and drivers
- **Driver :** Huge inverters to drive external loads
- **ESD clamp :** protects internal circuits of I/O and chip from zaps

Input buffer



- **Primary and Secondary ESD clamps :** Needed for efficient protection of devices from ESD
- **Weak pull-up/down :** To drive PAD to logic low/high to avoid static current in receiver.
- **Input stage :** buffers the external signal and decouples the external noise.
- **Level shifter :** limits the external signal level to core operating level.

Fig-4

Another typical requirement of many I/O buffer is to support higher voltage signaling at input, called tolerance. As technology advances, often some of the ICs with lower supply voltage are upgraded on a system. Let us take the example shown in Fig-5. Chip A and Chip B are modified to support 3.3V I/O supply whereas chip C still works at 5V I/O supply. If not properly protected, I/O buffers in Chip A and Chip B may fail as they see a voltage of 5V from Chip C. It is at this point, tolerant feature in an I/O buffer helps to achieve integrating different voltage domain chips but still maintaining full performance requirement.. There may be some cases where power might be turned off in one of the chips. Even under such circumstances, the device should not alter the overall performance or get damaged. To avoid this, a feature called fail-safe is added for many I/O buffers.

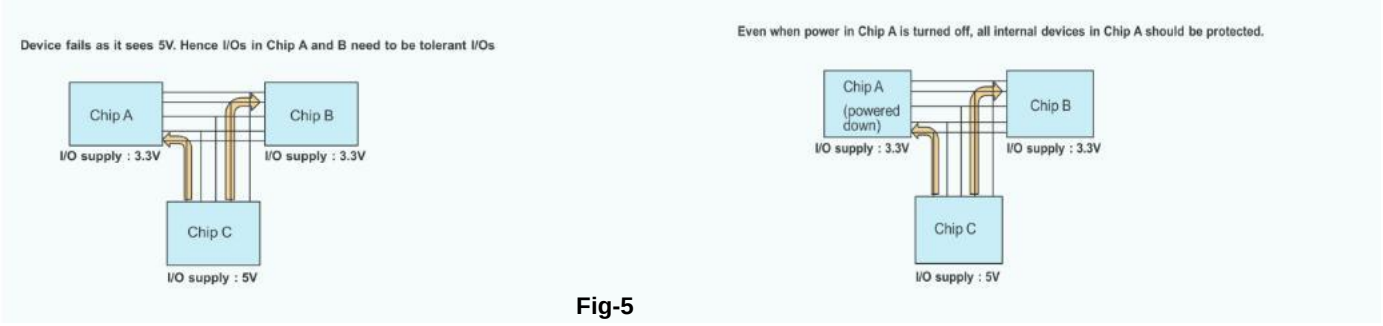


Fig-5

Many of the new technologies support lower voltage than required by legacy standards. IO design for such application requires stacking of transistor with proper biasing to avoid over-stress issues. LVDS and high speed IO designs require more involved analog circuits to meet electrical specifications.
As mentioned in Fig-6, stringent design methodology should be followed for I/O buffer design to weed out any issues later on. Design methodology starts with schematic design followed by layout. Layout for an I/O buffer requires more expertise to avoid Latch-up/ESD failures in the field.

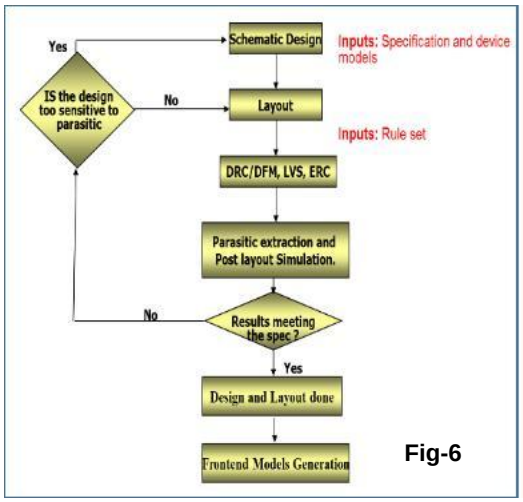


Fig-6

About KRIVI Semiconductor:

KRIVI is fast emerging as leading vendor for all types of IO pad libraries. Krivi have vast experience of developing first-time silicon pass IOs like GPIO,DDR, LPDDR, MIPI-RFFE, SDIO, high voltage special IO to differential like LVDS, Sub-LVDS, SLVS, UHS-2. Krivi also provides area optimized and leakage optimized customized IO libraries.
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