Understanding RF CMOS compact modeling to allow accurate RF & mm Wave circuit design

Bertrand Ardouin[1]

[1]XMOD Technologies, Bordeaux, France
* Email: ardouin@xmodtech.com

Abstract

This paper discusses the specific challenges which need to be solved in order to realize accurate RF CMOS compact modeling. By contrast to the standard baseband pure digital compact modeling work, RF CMOS modeling requires educated strategies in order to provide RF circuit designers with the level of confidence they expect from their EDA tools. The effort of building such strategies for device characterization, parameter extraction and final model Q/A (which is often underestimated) is the subject of this paper.

1. Introduction

With the constant decrease MOS transistor dimensions to keep up with Moore's law, the operating speed of CMOS processes has dramatically increased during the past years. This brought to the common view that pure CMOS solutions would always catch RF markets as soon as volume production is required. However, more recent process nodes have shown a decrease in MOSFET effective performance, especially with the impedance load typically found in RF and mm wave circuits [1]. Although intrinsic speed of 45nm MOSFETs transistors can reach the peak operating frequencies (f_T, f_{max}) of over 400GHz, it was demonstrated that it drops down to just 200GHz when the metallization necessary for building circuits is included [2]. This emphasizes the need for accurate and validated physics based compact models to gain the maximum performance of CMOS processes in the RF and mm wave domain.

2. Examples of critical characterization and modeling aspects

De-embedding RF pads parasitic elements is of utmost importance in order to obtain accurate measurements of the inner transistor. Several techniques have been developed, ranging from the simplest OPEN de-embedding to the very complex "6 dummies" de-embedding method [3]. Nevertheless, all these methods raise the common question of the reference plane. Actually, the OPEN and SHORT dummies structures ultimately determine the reference plane of the S parameters measurements, and one need to carefully and consistently design these critical test structures to properly set the modeling reference plane. Figure 1, shows various options to define the reference plane: top metal (1), intermediate (2) or first metal (3). Incorrect choice of the latter (e.g. with respect to the model choices and/or to the post layout parasitic extractor) can lead to several tens of GHz difference in the f_T and f_{max} determination.

Another critical aspect of RF MOS models is the need to accurately model the substrate parasitic network in order to correctly describe the transistor output conductance. Various parasitic substrate networks have been proposed in the literature with the emphasis on describing the observed measured data, but little effort has been spent on methodologies to remove the impact of self-heating on the apparent output conductance. Actually, for devices with large number of fingers, the self-heating effect and the thermal mutual coupling between transistor fingers leads to critical discrepancies between the DC and AC output conductance of the device. This phenomenon needs to be taken into account to accurately model S_{22}, for instance, a critical parameter for the design of any amplifier output matching network.

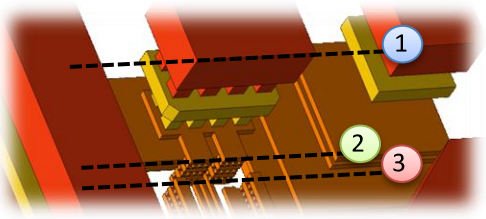

Figure 1. RF test structure: backend lines used to connect the transistor. De-embedding reference planes are shown

References

[1] S. Voinigescu et al., "A Study of SiGe HBT Signal Sources in the 220–330-GHz Range", IEEE J. of Solid-State Circuits, Vol. 48, No. 9, pp. 2011-2021, 2013.

[2] O. Inac et al., "Millimeter-Wave and THz Circuits in 45-nm SOI CMOS", Proc. CSICS, 4 pages, 2011.

[3] N. Derrier et al., "State-of-the-art and Future Perspectives in Calibration and De-Embedding Techniques for Characterization of Advanced SiGe HBTs featuring sub-THz f_T/f_{MAX}", BCTM 2012.